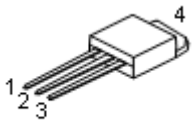
1. Description

This Power MOSFET is produced using KIA`s advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance,and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high effciency switched mode power supplies, active power factor correction based on half bridge topology.

2. Features

- $R_{DS(on)}$=130m Ω @ V_{GS}=10V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

3. Pin configuration



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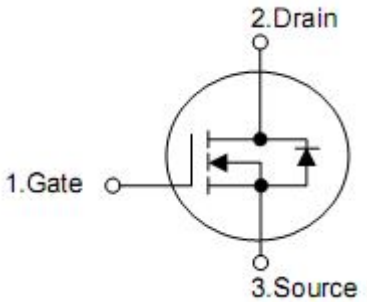

Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Absolutemaximum ratings

(T_C= 25 ºC, unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-source voltage	V_{DSS}	150	V
Gate-source voltage	V_{GSS}	±20	V
Drain current continuous	I_D	12	A
Drain current pulsed (note 1)	I_{DM}	50	A
Total power dissipation	P_D	55	W
Operating and storage temperature range	T_J, T_{STG}	-55~+175	ºC

5. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance,Junction-case (note 2)	R_{thJC}	2.7	ºC/W

6. Electrical characteristics

(T_C=25°C,unless otherwise noted)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Off characteristics							
Drain-source breakdown voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	150	-	-	V
Zero gate voltage drain current		I_{DSS}	V_{DS}=150V ,V_{GS}=0V	-	-	1	μA
Gate-body leakage current	Forward	I_{GSS}	V_{GS}=20V,V_{DS}=0V	-	-	100	nA
	Reverse		V_{GS}=-20V,V_{DS}=0V	-	-	-100	nA
On characteristics							
Gate threshold voltage		$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.5	2.0	2.5	V
Static drain-source on-resistance		$R_{DS(on)}$	V_{GS}=10V,I_D=5A	-	130	160	mΩ
Forward transconductance		g_{FS}	V_{DS}=15V,I_D=10A	-	15	-	S
Dynamic characteristics							
Input capacitance		C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1MHz	-	900	-	pF
Output capacitance		C_{oss}		-	115	-	pF
Reverse transfer capacitance		C_{rss}		-	70	-	pF
Switching characteristics							
Turn-on delay time		$t_{d(on)}$	V_{DD}=75V,I_D=1A, R_L=75Ω , V_{GS}=10V,R_{GEN}=6Ω	-	8	-	ns
Rise time		t_r		-	10	-	ns
Turn-off delay time		$t_{d(off)}$		-	20	-	ns
Fall time		t_f		-	15	-	ns
Total gate charge		Q_g	V_{DS}=75V,I_D=1.5A , V_{GS}=10V	-	19	-	nC
Gate-source charge		Q_{gs}		-	5.5	-	nC
Gate-drain charge		Q_{gd}		-	7	-	nC
Drain-source diode characteristics and maximum ratings							
Drain-source diode forward voltage(note 3)		V_{SD}	V_{GS}=0V,I_{SD}=12A	-	-	1.2	V
Continuous drain-source current (note 2)		I_{SD}		-	-	12	A

Notes: 1.Repetitive rating: pulse width limited by maximum junction temperature

2. Surface mounted on FR4 board, t ≤10sec.

3. Pulse test: pulse width≤300μs, duty cycle≤2%

4. Guaranteed by design, not subject to production

7. Test circuits and waveforms

Typical Electrical and Thermal Characteristics (Curves)

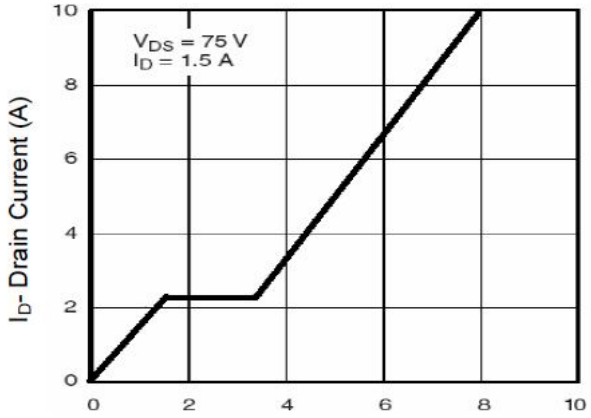

Figure 1 Output Characteristics

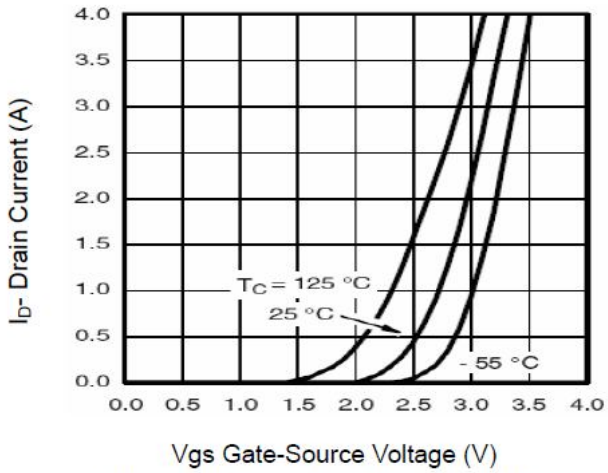

Figure 2 Transfer Characteristics

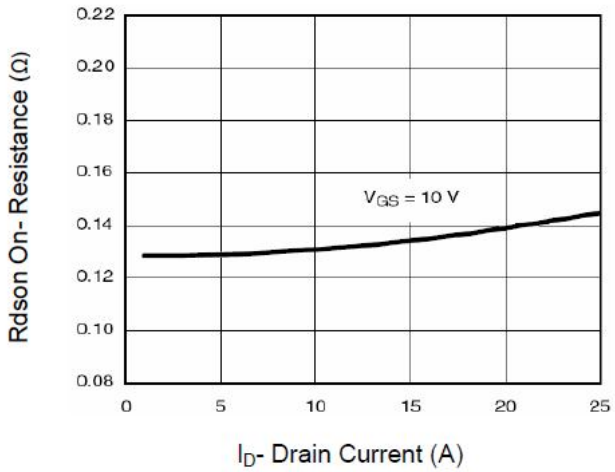

Figure 3 Rdson- Drain Current

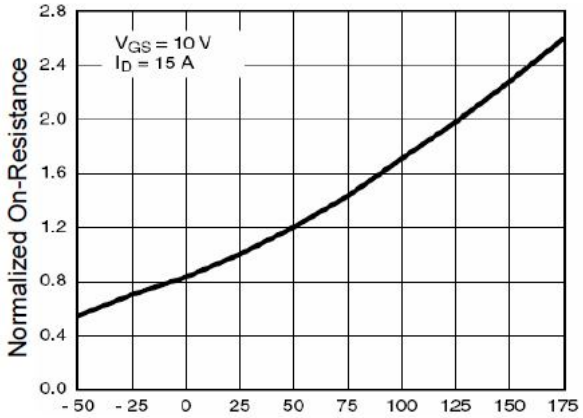

Figure 4 Rdson- Junction Temperature

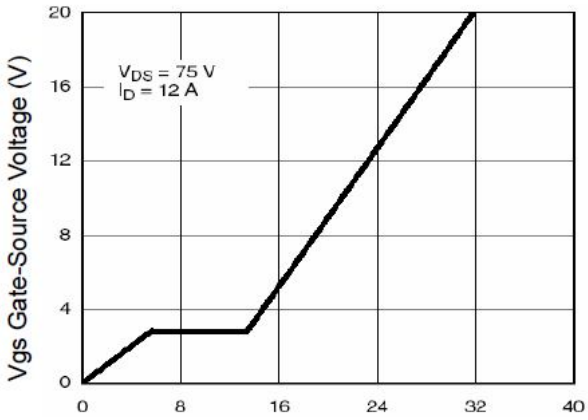

Figure 5 Gate Charge

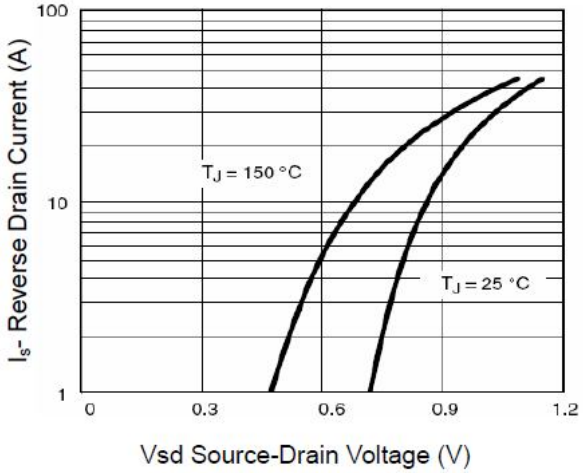

Figure 6 Source- Drain Diode Forward

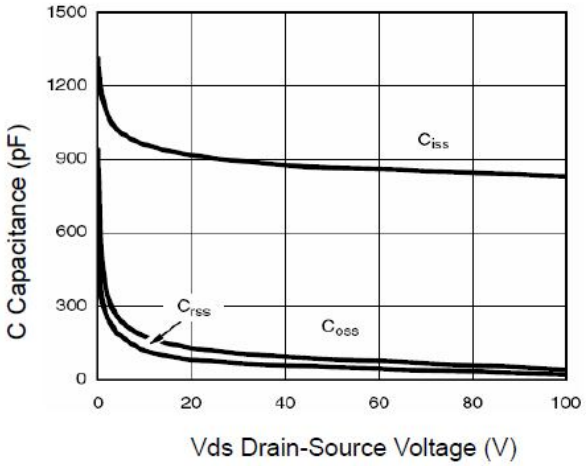

Figure 7 Capacitance vs Vds

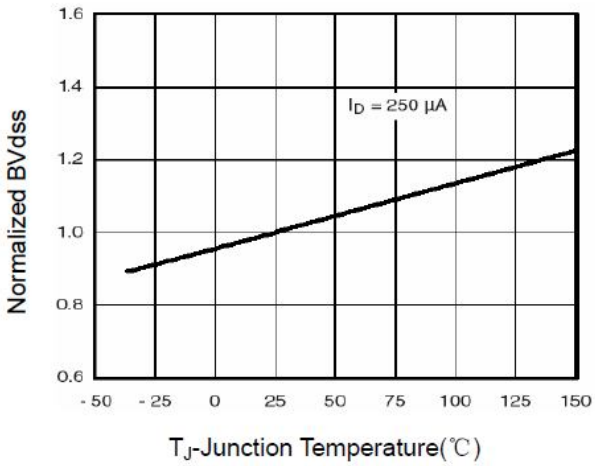

Figure 9 BV_{DSS} vs Junction Temperature

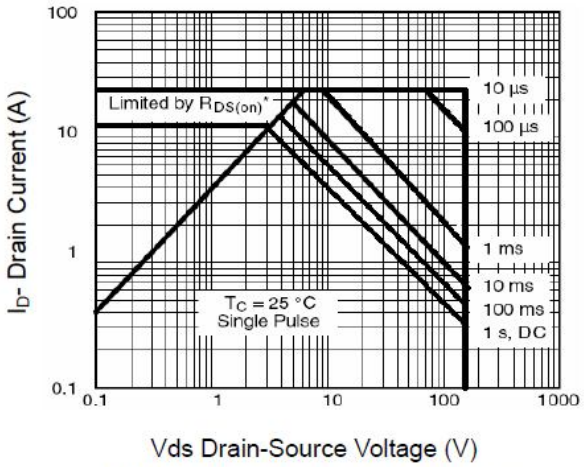

Figure 8 Safe Operation Area

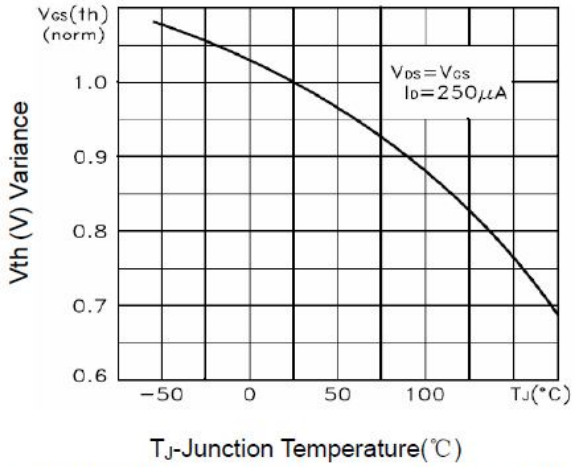

Figure 10 $V_{GS(th)}$ vs Junction Temperature

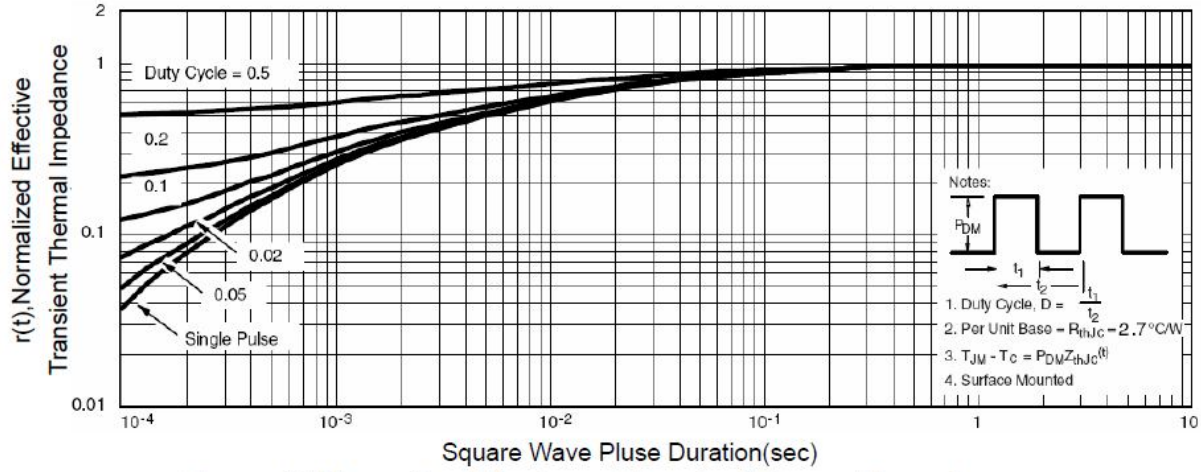

Figure 11 Normalized Maximum Transient Thermal Impedance