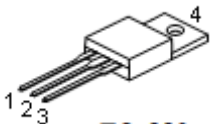
1. Features

- Proprietary New Planar Technology
- $R_{DS(ON)}$=50m Ω(typ.)@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

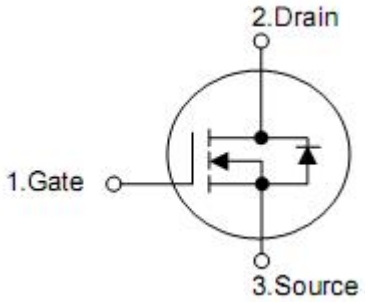
2. Application

- DC-DC Converters
- DC-AC Inverters for UPS
- SMPS and Motor controls

3. Pin configuration



TO-220



Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Ordering Information

Part Number	Package	Brand
KNP9120A	TO-220	KIA

5. Absolute maximum ratings

(T_C= 25ºC , unless otherwise specified)

Parameter		Symbol	Rating	Units
Drain-source voltage[1]		V_{DSS}	200	V
Gate-source voltage		V_{GSS}	±20	V
Continuous Drain Current		I_D	40	A
Continuous Drain Current @Tc=100ºC		$I_{D\ @\ TC=100ºC}$	Figure3	A
Pulsed Drain Current at V_{GS}=10V[2]		I_{DM}	Figure6	A
Avalanche energy	Single pulse	E_{AS}	1200	mJ
Peak Diode Recovery dv/dt[3]		dv/dt[3]	5.0	V/ns
Power Dissipation		P_D	125	W
Derating Factor above 25 ºC			1.0	W/ºC
Maximum Temperature for Soldering Leads at 0.063in(1.6mm) form Case for 10 Seconds		T_L T_{PAK}	300 260	ºC
Storage temperature		T_{STG}	-55~+150	ºC

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

6. Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.0	ºC/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	

7. Electrical characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Off characteristics		(T_J=25°C,unless otherwise specified)				
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	200	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=200V ,V_{GS}=0V	-	-	1	μA
		V_{DS}=160V , V_{GS}=0V T_J=125 ºC	-	-	100	μA
Gate-to-source Leakage Current	I_{GSS}	V_{GS}=+20V, V_{DS}=0V	-	-	+100	nA
		V_{GS}=-20V, V_{DS}=0V	-	-	-100	nA
On characteristics		(T_J=25°C,unless otherwise specified)				
Gate threshold voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2.0	-	4.0	V
Static drain-source on-resistance	$R_{DS(ON)}$	Vg_S=10V,I_D=20A	-	50	65	mΩ
Forward Transconductance[4]	G_{FS}	V_{DS}=15V,I_D=20A	-	65	-	S
Dynamic characteristics		(Essentially independent of operating temperature)				
Input capacitance	C_{ISS}	V_{DS}=25V,V_{GS}=0V, f=1.0 MHz	-	2800	3700	pF
Output capacitance	C_{OSS}		-	305	400	pF
Reverse transfer capacitance	C_{RSS}		-	110	150	pF
Turn-on delay time	$t_{D(ON)}$	V_{DD}=100V,I_D=20A, R_G=3.9Ω,VGS=10V	-	20	-	ns
Rise time	t_R		-	30	-	ns
Turn-off delay time	$t_{D(OFF)}$		-	65	-	ns
Fall time	t_F		-	25	-	ns
Switching characteristics		(Essentially independent of operating temperature)				
Total gate charge	Q_G	V_{DD}=100V, I_D=20A V_{GS}=0 to10V	-	97	120	nC
Gate-source charge	Q_{GS}		-	14	-	nC
Gate-drain charge	Q_{GD}		-	39	-	nC
Switching characteristics		(T_J=25°C,unless otherwise specified)				
Drain-source diode forward voltage	V_{SD}	V_{GS}=0V, I_S=40A	-	-	1.5	V
Continuous drain-source current[4]	I_{SD}	Integral PN-diode in MOSFET	-	-	40	A
Pulsed drain-source current[4]	I_{SM}		-	-	160	A
Reverse recovery time	t_{rr}	V_{GS}=0V,I_F=20A di_F/dt=100A/μs	-	280	-	ns
Reverse recovery charge	Q_{rr}		-	420	-	μC

NOTE:[1] TJ=+25ºC to +150ºC ;
[2] Repetitive rating; pulse width limited by maximum junction temperature;
[3] ISD= 20A di/dt < 100 A/μs, VDD < BVDSS, TJ=+150ºC;
[4] Pulse width≤380μs; duty cycle≤2%.

8. Test circuits and waveforms

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

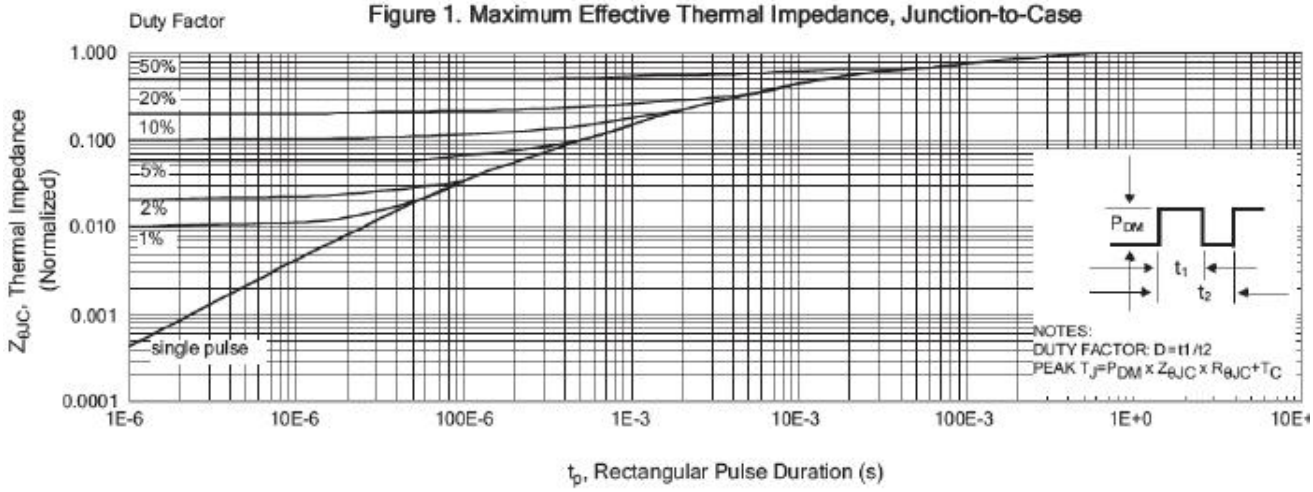


Figure 2. Maximum Power Dissipation vs Case Temperature

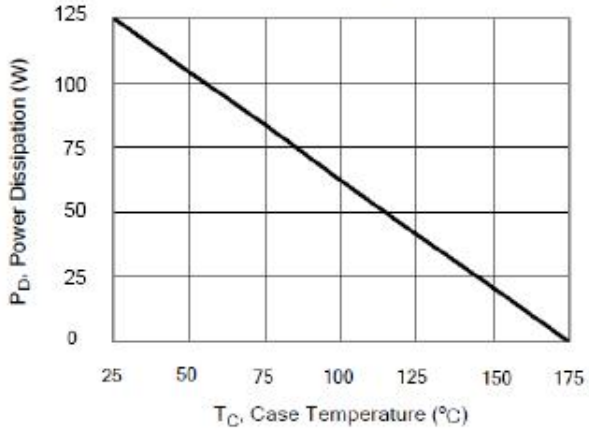


Figure3. Maximum Continuous Drain Current vs Case Temperature

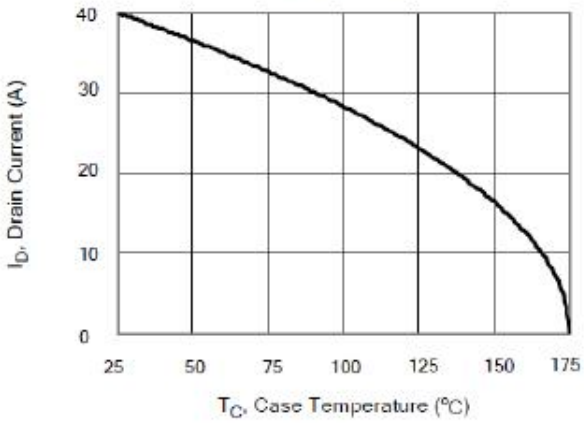


Figure 4. Typical Output Characteristics

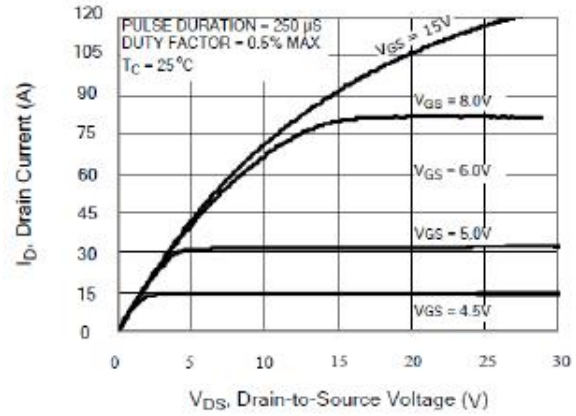


Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

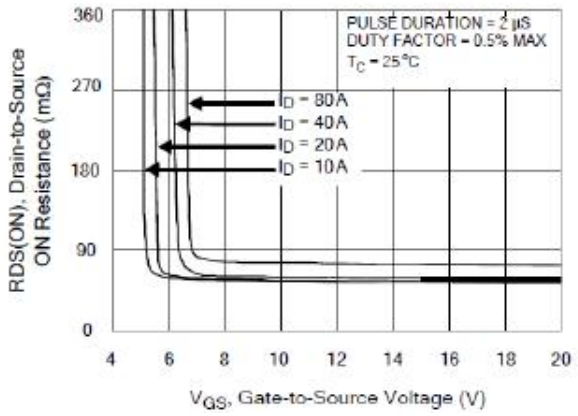


Figure 6. Maximum Peak Current Capability

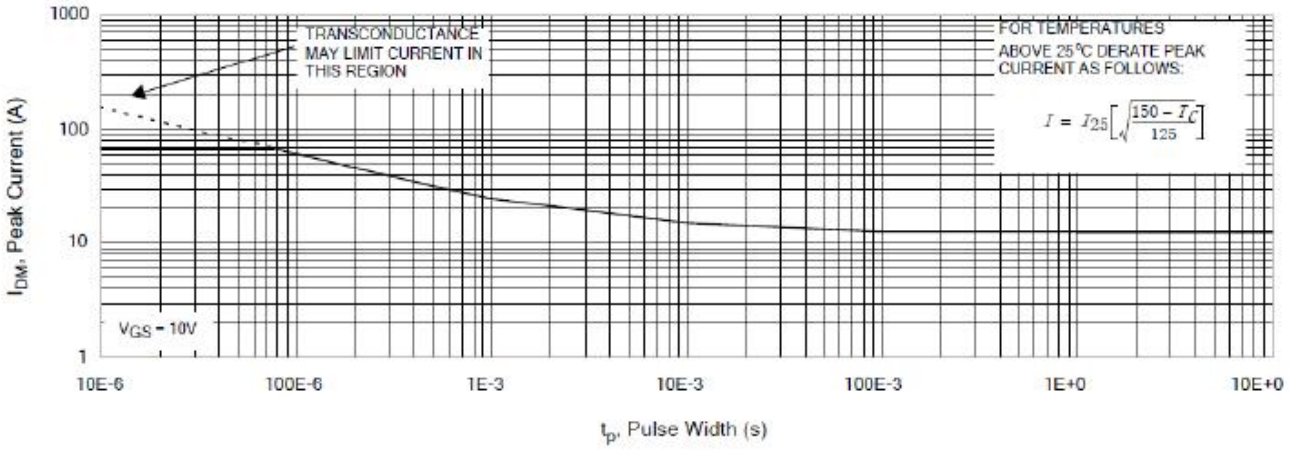


Figure 7. Typical Transfer Characteristics

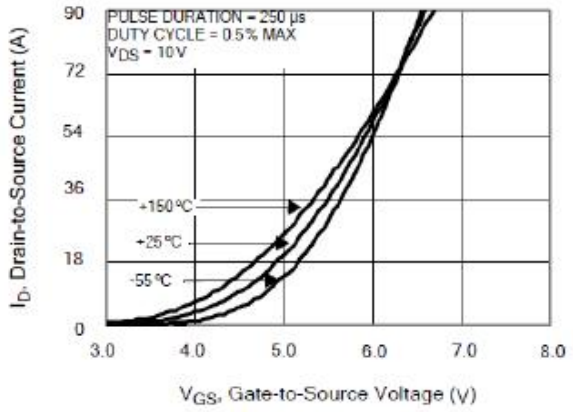


Figure 8. Unclamped Inductive Switching Capability

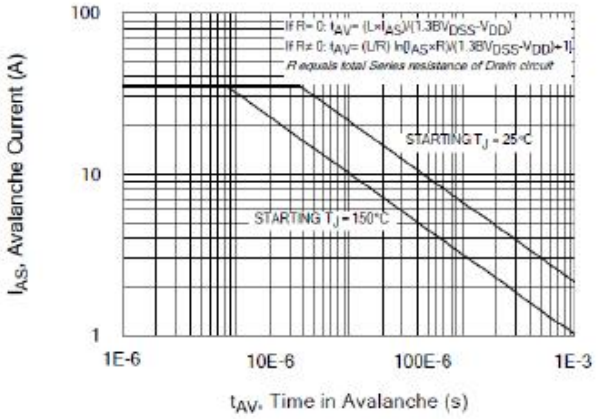


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

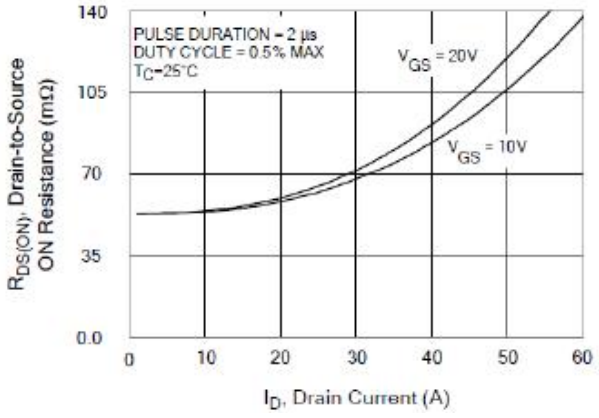


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

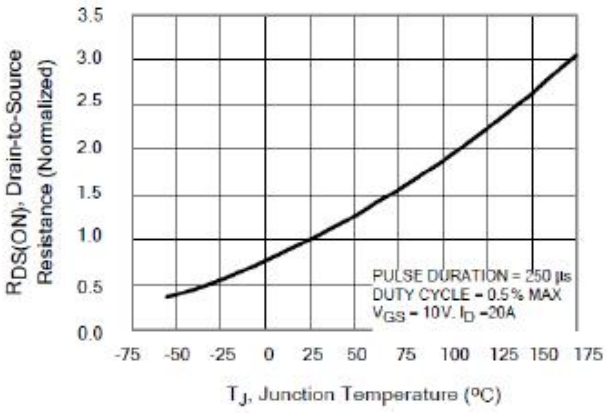


Figure 11. Typical Breakdown Voltage vs Junction Temperature

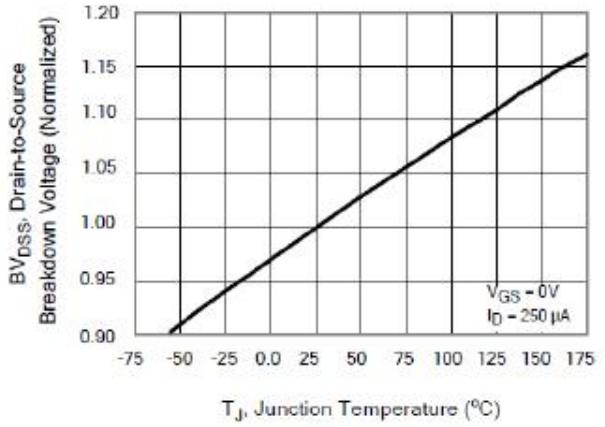


Figure 12. Typical Threshold Voltage vs Junction Temperature

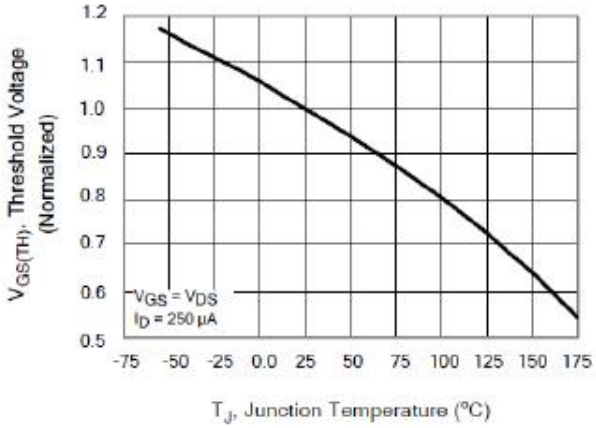


Figure 13. Maximum Forward Bias Safe Operating Area

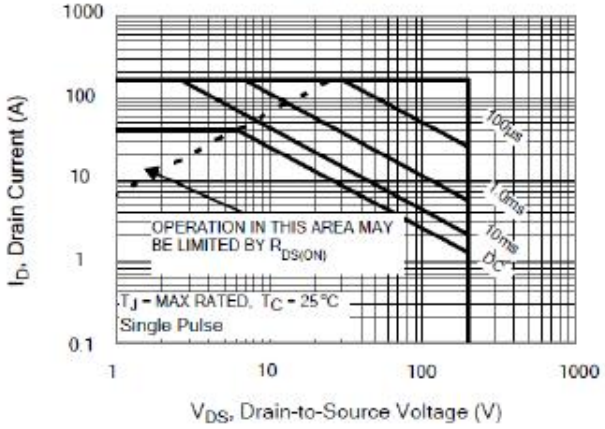


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

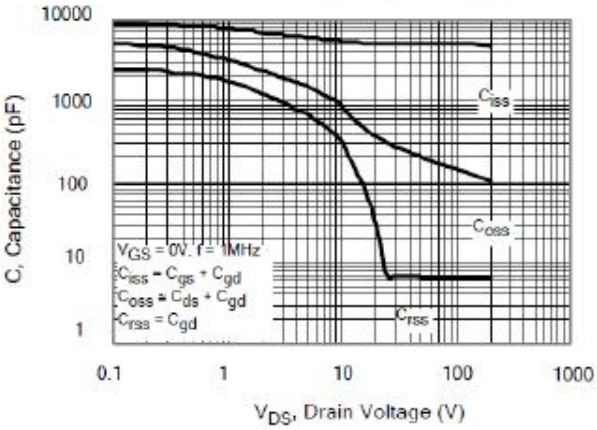


Figure 15 .Typical Gate Charge

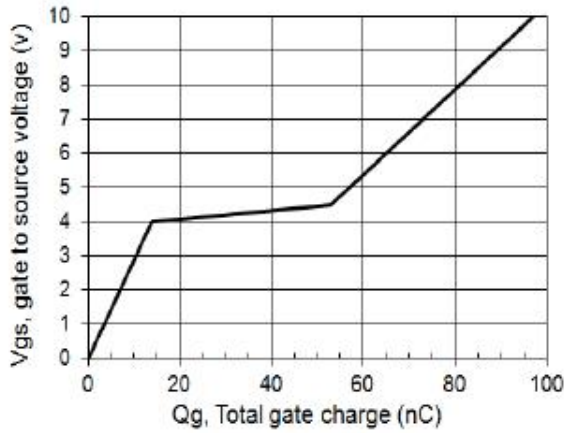
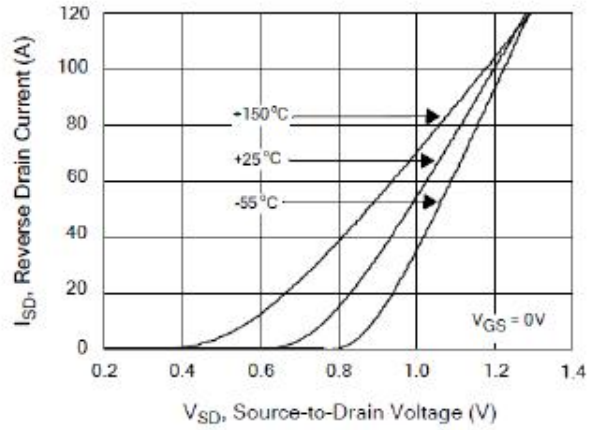


Figure 16. Typical Body Diode Transfer Characteristics



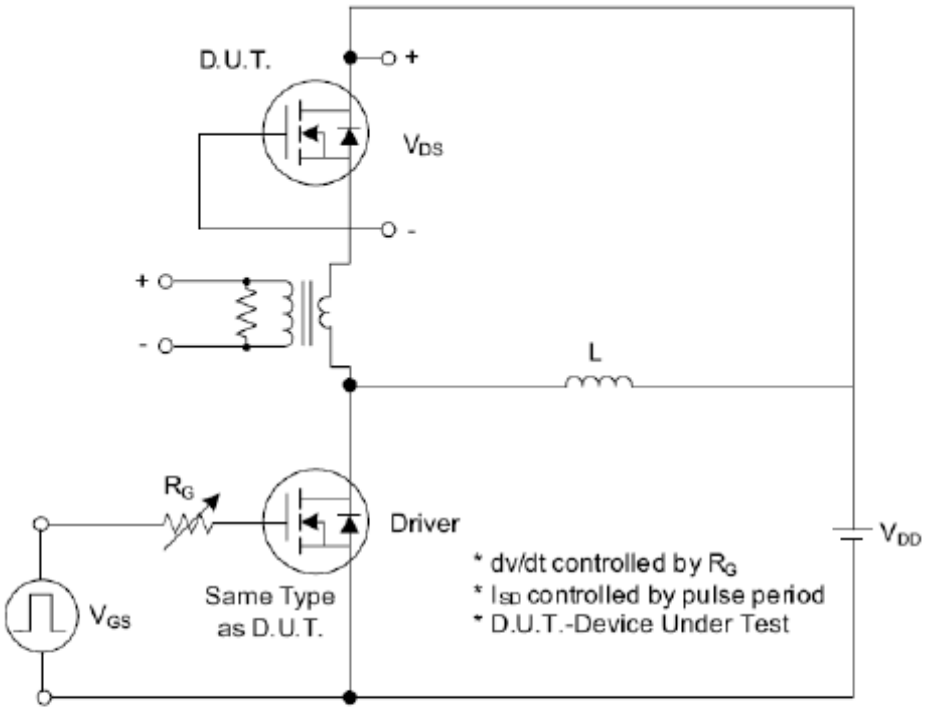


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

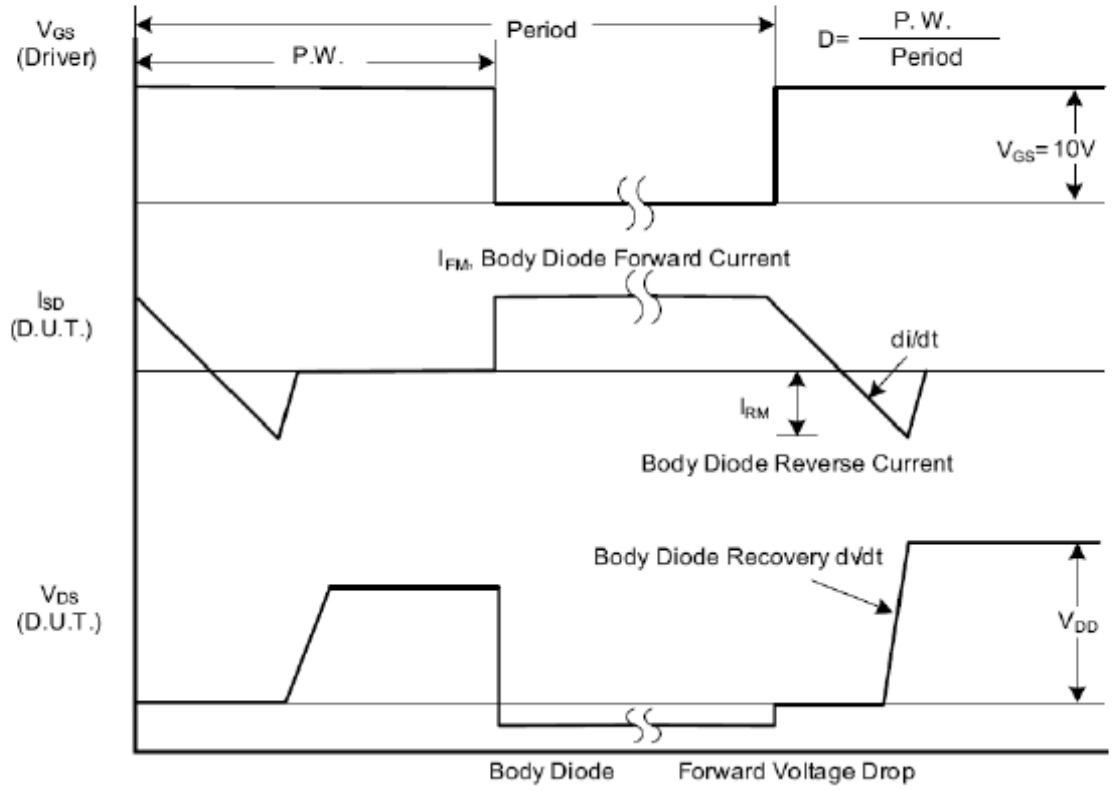


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

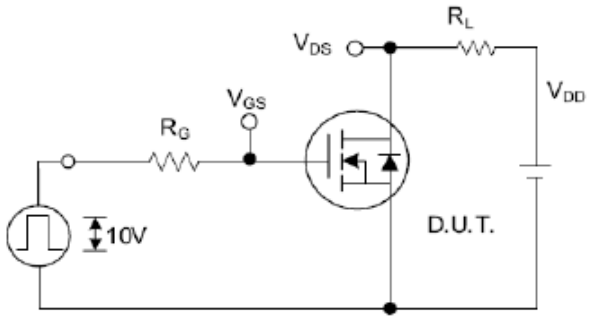


Fig. 2.1 Switching Test Circuit

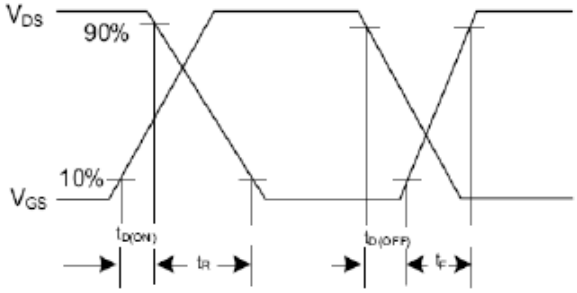


Fig. 2.2 Switching Waveforms

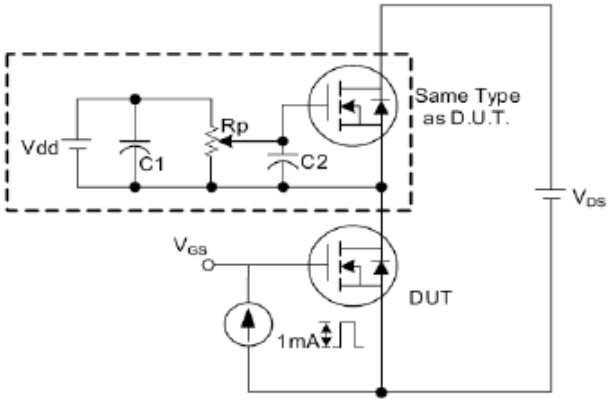


Fig. 3 . 1 Gate Charge Test Circuit

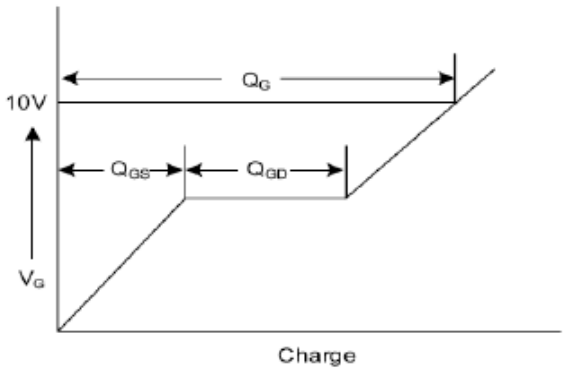


Fig. 3 . 2 Gate Charge Waveform

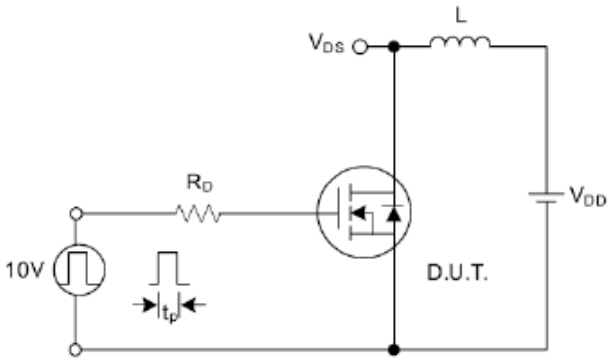


Fig. 4.1 Unclamped Inductive Switching Test Circuit

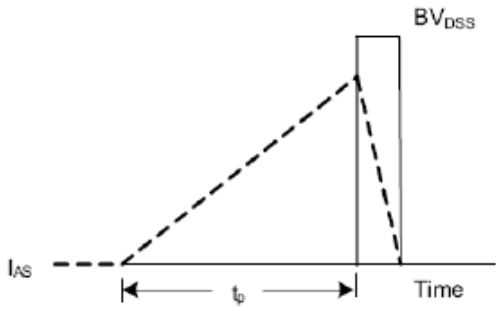


Fig. 4.2 Unclamped Inductive Switching Waveforms