

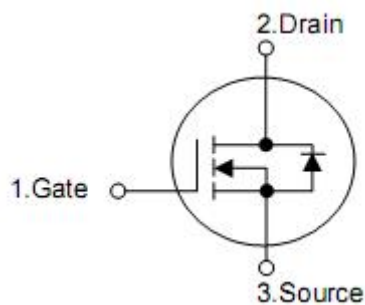
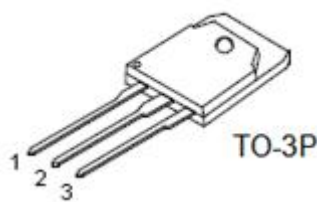
1. Description

This Power MOSFET is produced using KIA advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

2. Features

- n $R_{DS(on)}=0.17\Omega @ V_{GS}=10V$
- n Low gate charge (typical 102nC)
- n Fast switching capability
- n Avalanche energy specified
- n Improved dv/dt capability

3. Pin configuration



Pin	Function
1	Gate
2	Drain
3	Source

4. Absolute maximum ratings

(T_C= 25 °C , unless otherwise specified)

Parameter	Symbol	Ratings	Units	
Drain-source voltage	V _{DSS}	500	V	
Gate-source voltage	V _{GSS}	+30	V	
Drain current continuous	I _D	T _C =25°C	28	A
		T _C =100°C	16.8	A
Drain current pulsed (note1)	I _{DP}	112	A	
Avalanche energy	E _{AR}	Repetitive (note1)	43	mJ
		Single pulse (note2)	1960	mJ
Peak diode recovery dv/dt (note 3)	dv/dt	4.5	V/ns	
Total power dissipation	P _D	T _C =25°C	479	W
		derate above 25°C	3.83	W/°C
Junction temperature	T _J	+150	°C	
Storage temperature	T _{STG}	-55~+150	°C	

*Drain current limited by maximum junction temperature.

5. Thermal characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance,junction-ambient	R _{thJA}	62.5	°C/W
Thermal resistance,case-to-sink typ.	R _{thCS}	0.5	
Thermal resistance,Junction-case	R _{thJC}	0.26	

6. Electrical characteristics

(T_J=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Off characteristics							
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	500	-	-	V	
Zero gate voltage drain current	I _{DSS}	V _{DS} =500V, V _{GS} =0V	-	-	1	μA	
		V _{DS} =400V, T _C =125 °C	-	-	10	μA	
Gate-body leakage current	Forward	I _{GSS}	V _{GS} =30V, V _{DS} =0V	-	-	100	nA
	Reverse					-100	nA
Breakdown voltage temperature coefficient	ΔBV _{DSS} /ΔT _J	I _D =250μA	-	0.6	-	V/°C	
On characteristics							
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0	-	4.0	V	
Static drain-source on-resistance	R _{DS(on)}	V _{GS} =10V, I _D =14A	-	0.16	0.2	Ω	
Forward transconductance	g _{FS}	V _{DS} =40V, I _D =14A (note4)	-	26	-	S	
Dynamic characteristics							
Input capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHz	-	4085	-	pF	
Output capacitance	C _{oss}		-	474	-	pF	
Reverse transfer capacitance	C _{rss}		-	60	-	pF	
Switching characteristics							
Turn-on delay time	t _{d(on)}	V _{DD} =250V, I _D =28A, R _G =25Ω (note4,5)	-	45	-	ns	
Rise time	t _r		-	87	-	ns	
Turn-off delay time	t _{d(off)}		-	355	-	ns	
Fall time	t _f		-	130	-	ns	
Total gate charge	Q _g	V _{DS} =400V, I _D =28A, V _{GS} =10V (note4,5)	-	102	-	nC	
Gate-source charge	Q _{gs}		-	43	-	nC	
Gate-drain charge	Q _{gd}		-	20	-	nC	
Drain-source diode characteristics							
Drain-source diode forward voltage	V _{SD}	V _{GS} =0V, I _D =28A	-	-	1.4	V	
Continuous drain-source current	I _{SD}		-	-	28	A	
Pulsed drain-source current	I _{SM}		-	-	112	A	
Reverse recovery time	t _{rr}	I _{SD} =28A di _{SD} /dt=100A/μs (note4)	-	656	-	ns	
Reverse recovery charge	Q _{rr}		-	11.5	-	μC	

Note: 1 Repetitive rating: pulse width limited by maximum junction temperature

2. L=5mH, I_{AS}=28A, V_{DD}=50V, R_G=25Ω, starting T_J=25°C
3. I_{SD}≤28A, di/dt≤100A/μs, V_{DD}≤BV_{DSS}, starting T_J=25 °C
4. Pulse test: pulse width≤300μs, duty cycle≤2%
5. Essentially independent of operating temperature

7. Test circuits and waveforms

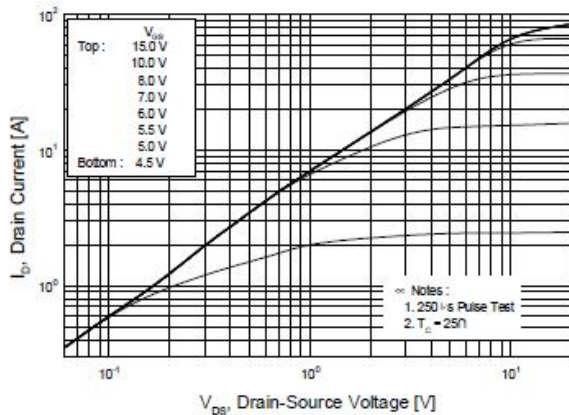


Figure 1. On-Region Characteristics

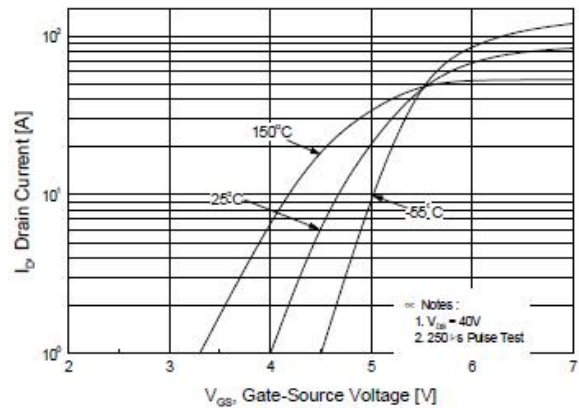


Figure 2. Transfer Characteristics

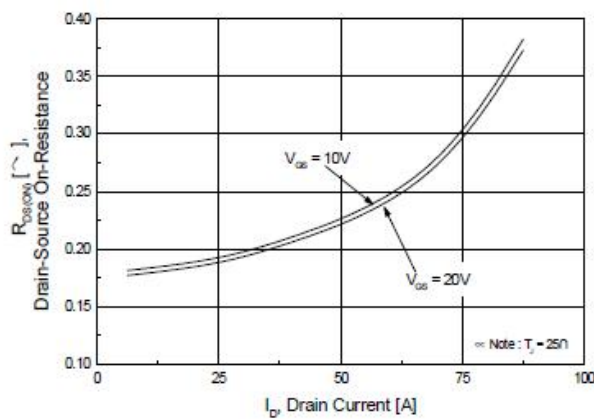


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

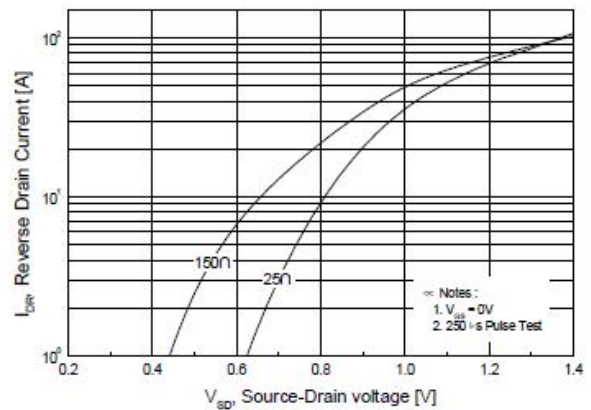


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

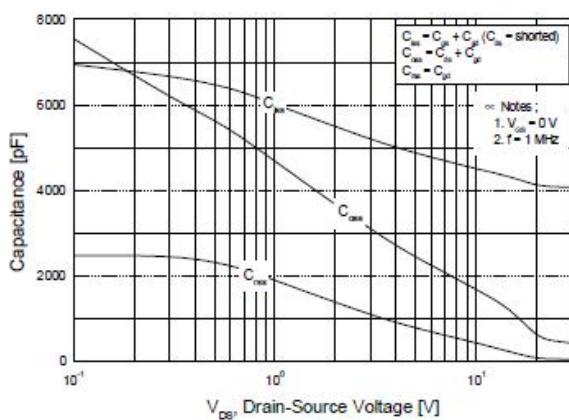


Figure 5. Capacitance Characteristics

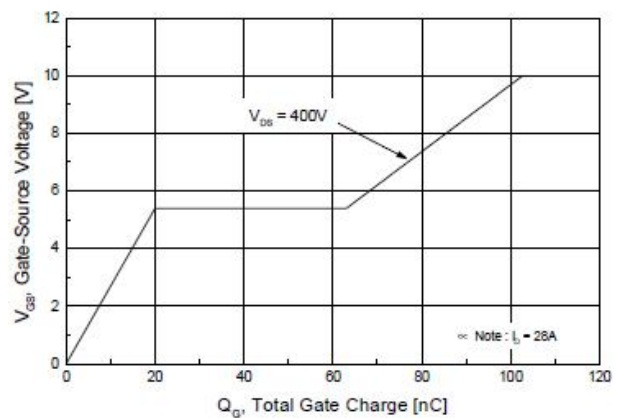


Figure 6. Gate Charge Characteristics

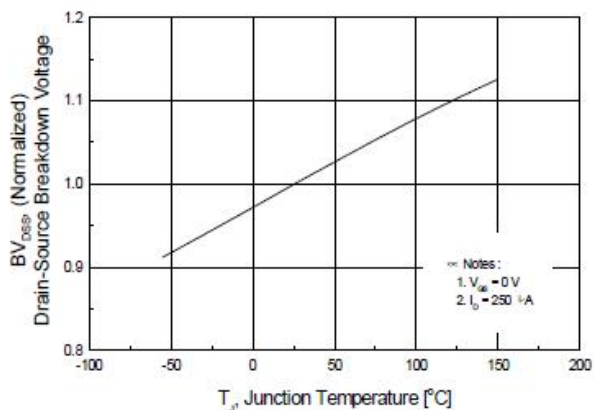


Figure 7. Breakdown Voltage Variation vs Temperature

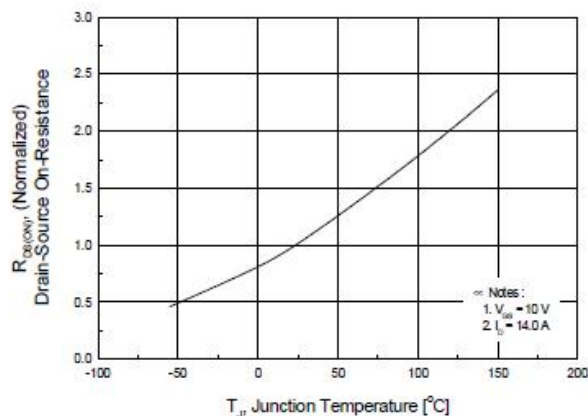


Figure 8. On-Resistance Variation vs Temperature

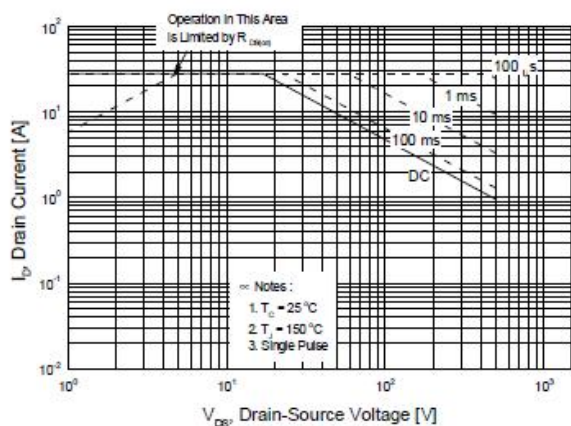


Figure 9. Maximum Safe Operating Area

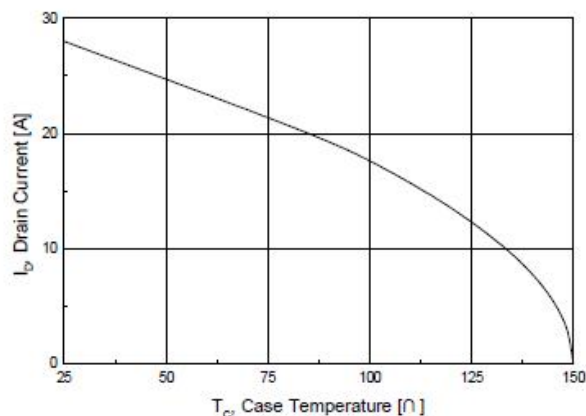


Figure 10. Maximum Drain Current vs Case Temperature

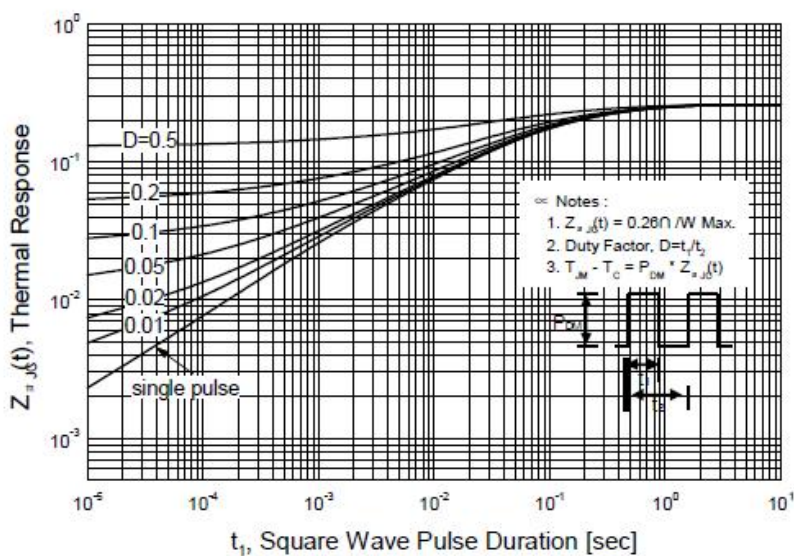


Figure 11. Transient Thermal Response Curve