

## 1. Description

The KIA3302A uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a wide variety of applications.

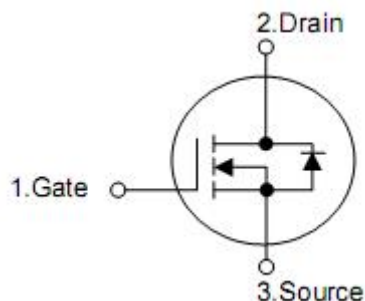
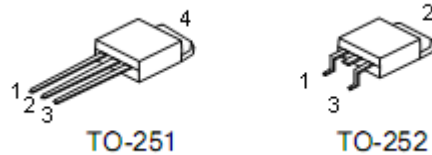
## 2. Features

- n  $R_{DS(on)}=3.9m\Omega$  @  $V_{DS}=4.5V$
- n High power and current handing capability
- n Lead free product is acquired
- n Surface mount package

## 3. Applications

- n Battery protection
- n Load switch
- n Power management

## 4. Symbol



Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

## 5. Absolute maximum ratings

Parameter	Symbol	Rating	Units
Drain-source voltage	$V_{DS}$	20	V
Gate-source voltage	$V_{GS}$	$\pm 12$	V
Continuous drain current, $V_{GS}$ @10V	$I_D$	$T_C=25^{\circ}C^1$	A
		$T_C=100^{\circ}C$	A
Pulsed drain current <sup>2</sup>	$I_{DM}$	340	A
Single pulse avalanche energy <sup>3</sup>	$E_{AS}$	340	mJ
Total power dissipation	$P_D$	$T_C=25^{\circ}C$	W
Total power dissipation		$T_C=100^{\circ}C$	W
Operation junction temperature range	$T_J$	-55 to175	$^{\circ}C$
Storage temperature range	$T_{STG}$	-55 to175	$^{\circ}C$

## 6. Thermal characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal resistance,Junction-case	$R_{\theta JC}$	--	1.72	$^{\circ}C/W$

## 7. Electrical characteristics

(T<sub>A</sub>=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	20	25	-	V
Static drain-source on-resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A T <sub>C</sub> =25°C	-	3.9	5.5	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =15A T <sub>C</sub> =25°C	-	6	9	
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A T <sub>C</sub> =125°C	-	5.4	8	
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =15A	-	6	9	
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.5	0.7	1.1	V
Drain-source leakage current	I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	-	-	1	μA
Gate- source leakage current	I <sub>GSS</sub>	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V	-	-	±100	nA
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =15A	-	40	-	S
Gate resistance	R <sub>g</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	-	1.1	-	Ω
Total gate charge(4.5V)	Q <sub>g</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> =4.5V I <sub>D</sub> =12A	-	32	-	nC
Gate-source charge	Q <sub>gs</sub>		-	3	-	
Gate-drain charge	Q <sub>gd</sub>		-	11	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DS</sub> =15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω, V <sub>GS</sub> =4.5V	-	17	-	ns
Rise time	t <sub>r</sub>		-	49	-	
Turn-off delay time	t <sub>d(off)</sub>		-	74	-	
Fall time	t <sub>f</sub>		-	26	-	
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	-	2800	-	pF
Output capacitance	C <sub>oss</sub>		-	353	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	265	-	
Source-drain current(Body diode)	I <sub>SD</sub>		-	-	85	A
Diode forward voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	-	-	1.2	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>f</sub> =20A. dI/dt=100A/us	-	23	-	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	10	-	nC

Note:1.The maximum current rating is package limited

2.Repetitive rating: pulse width limited by maximum junction temperature.

3.EAS condition: T<sub>J</sub>25°C, V<sub>DD</sub>=30V, V<sub>G</sub>=4.5V, R<sub>G</sub>=25Ω.

8. Test circuits

Figure 1. Output Characteristics

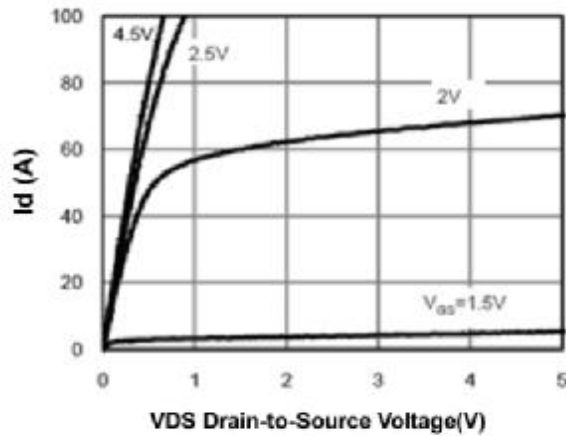


Figure 2. Transfer Characteristics

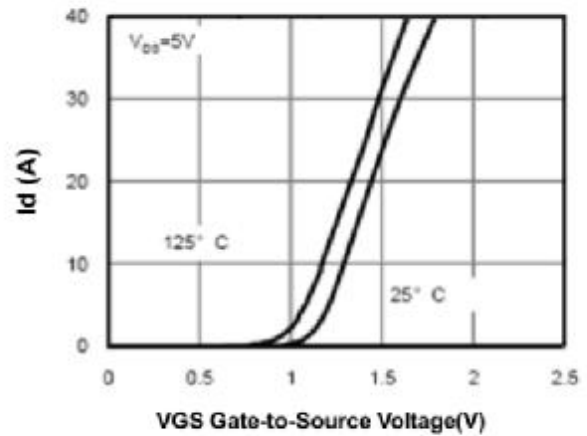


Figure 3. Max BV<sub>DSS</sub> vs Junction Temperature

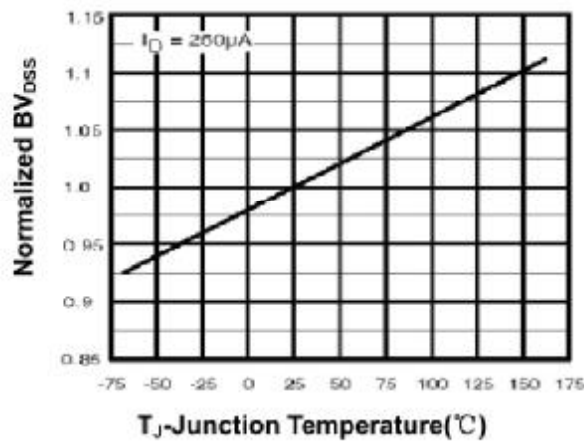


Figure 4. Drain Current

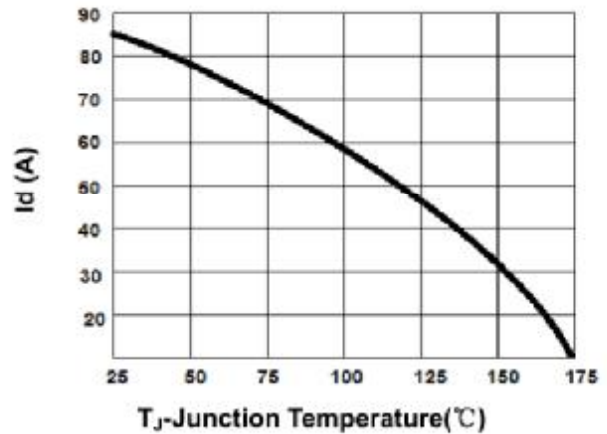


Figure 5. V<sub>GS(th)</sub> vs Junction Temperature

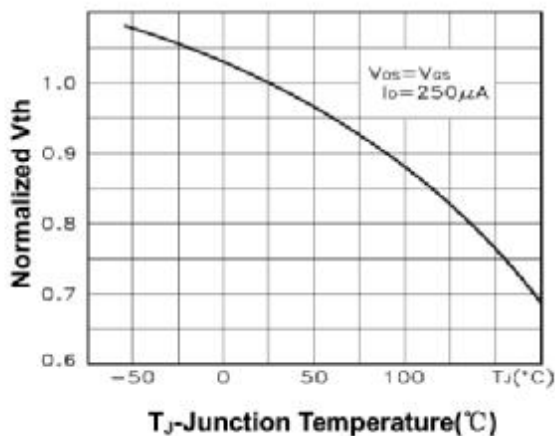


Figure 6. R<sub>DS(ON)</sub> vs Junction Temperature

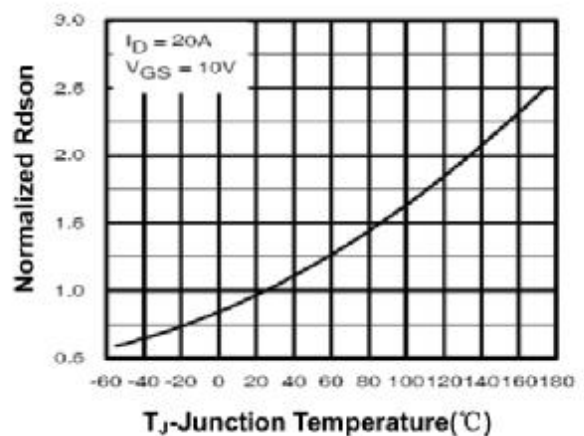


Figure 7. Gate Charge Waveforms

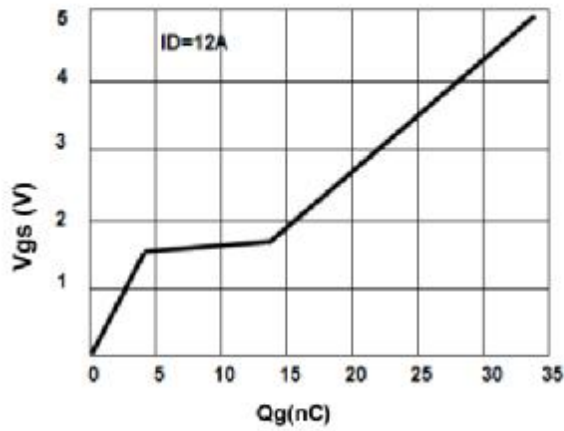


Figure 8. Capacitance

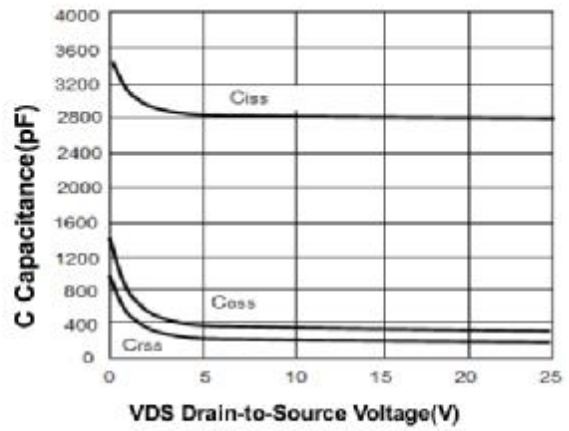


Figure 9. Body-Diode Characteristics

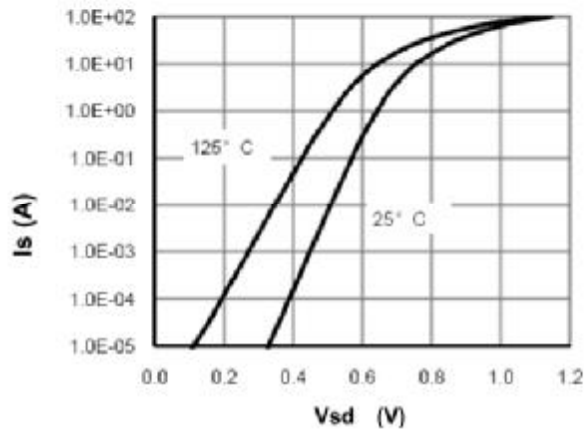


Figure 10. Maximum Safe Operating Area

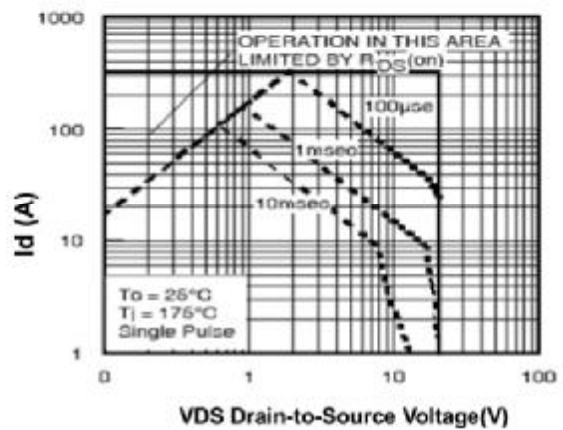


Figure 11. Normalized Maximum Transient Thermal Impedance

