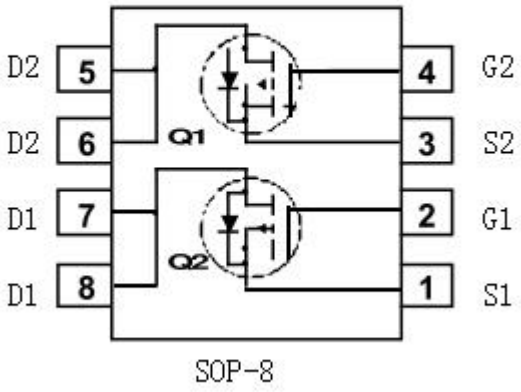
1. Features

- -30V/-5.3A,RDS(on) =54mΩ(typ)(Vgs =-10V)
  RDS(on) =84mΩ(Vgs=-4.5V)
- Low gate charge (6nC typical)
- High power and current handling capability
- Fast switching speed

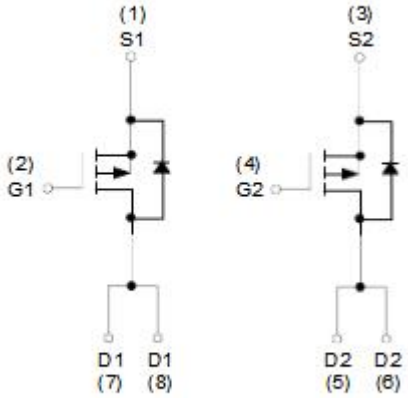
2.Applications

This Dual P-Channel MOSFET is a rugged gate version of KIA 's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gave drive voltage ratings (4.5V – 20V).

3.Symbol



SOP-8



P-Channel MOSFET

4. Absolute maximum ratings

Parameter		Symbol	Rating	Units
Drain-source voltage		V_{DSS}	-30	V
Gate-source voltage		V_{GS}	±20	V
Maximum drain current - continuous	T_C=25°C	I_D	-5.3	A
Maximum drain current- pulsed		I_{DM}	-20	
Maximum power dissipation (note 1)	T_C=25°C	P_D	2	W
	T_A=100°C		1	
Junction and storage temperature range		T_J ,T_{STG}	-55 to150	°C
Thermal resistance-junction to ambient (note 1)		$R_{\theta JA}$	78	°C/W
Thermal resistance-junction to Case (note 1)		$R_{\theta JC}$	40	°C/W

5. Electrical characteristics

(T_J=25°C,unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Static						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	-30	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=24V, V_{GS}=0V	-	-	-1	μA
Gate-source forward leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS}= V_{GS},I_D=250uA	-1.0	-1.7	-3.0	V
Drain-source on-state resistance [2]	$R_{DS(on)}$	V_{GS}=-10V,I_D=-5.3A	-	54	59	mΩ
		V_{GS}=-4.5V,I_D=-4.2A	-	84	89	
Diode forward voltage[2]	V_{SD}	V_{GS}=0V,I_S=-3A	-	-0.8	-1.28	V
Dynamic [1]						
Total gate charge(4.5V)	Q_g	V_{DS}=-15V,V_{GS}=-5V ID=-5A	-	6.0	-	nC
Gate-source charge	Q_{gs}		-	2.2	-	
Gate-drain charge	Q_{gd}		-	2.0	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=-15V,R_{GEN}=6Ω V_{GS}=-10V,I_D=-1A	-	7	-	ns
Rise time	t_r		-	13	-	
Turn-off delay time	$t_{d(off)}$		-	14	-	
Fall time	t_f		-	9	-	
Input capacitance	C_{iss}	V_{GS}=0V,V_{DS}=-15V f=1MHz	-	525	-	pF
Output capacitance	C_{oss}		-	130	-	
Reverse transfer capacitance	C_{rss}		-	70	-	

Notes:

1.Guaranteed by design, not subject to production testing

2.Pulse test ; pulse width ≤300μs, duty cycle ≤ 2%

3.$R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.$R_{\theta JC}$ is guaranteed by design while $R_{\theta JC}$ is determined by the user's board design.

6. Typical operating characteristics

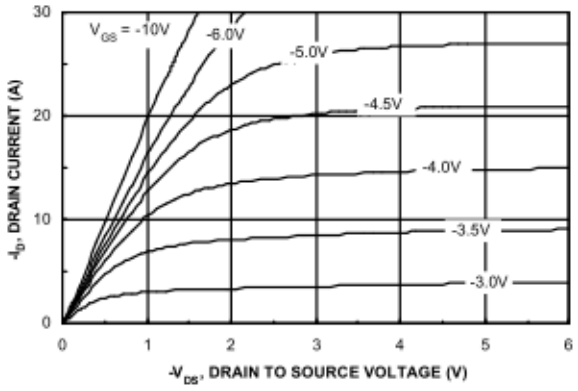


Figure 1. On-Region Characteristics.

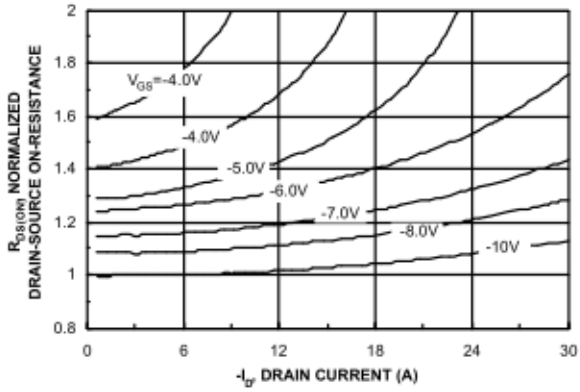


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

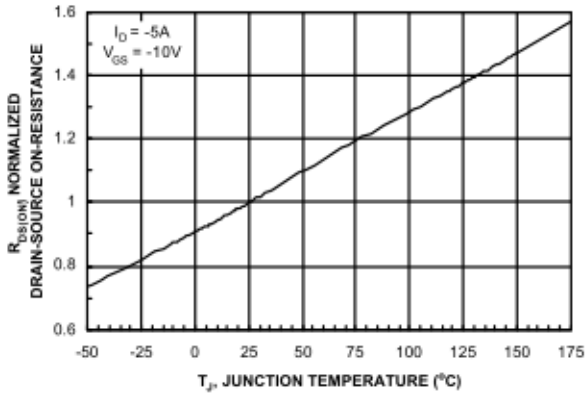


Figure 3. On-Resistance Variation with Temperature.

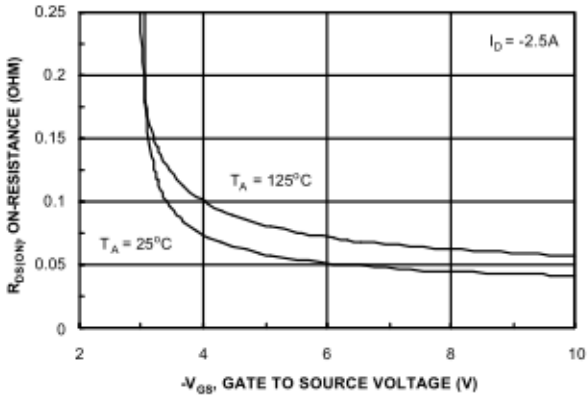


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

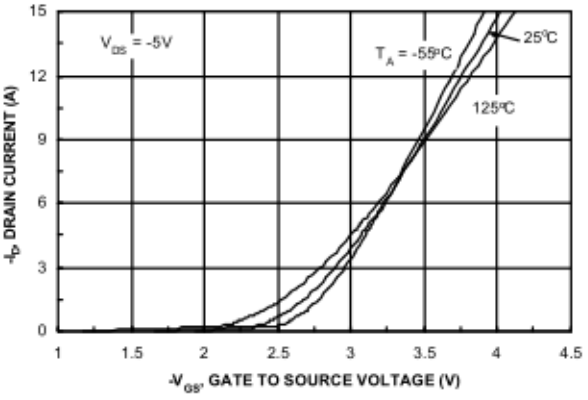


Figure 5. Transfer Characteristics.

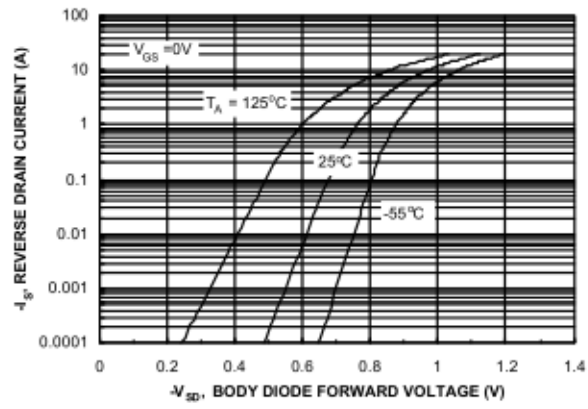


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

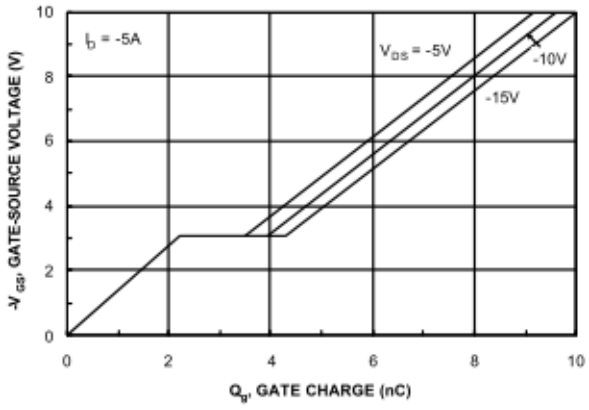


Figure 7. Gate Charge Characteristics.

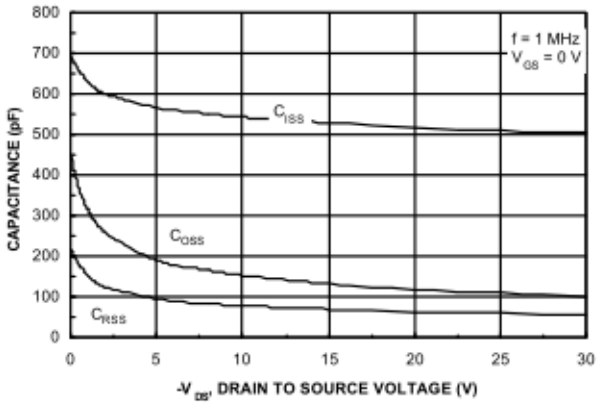


Figure 8. Capacitance Characteristics.

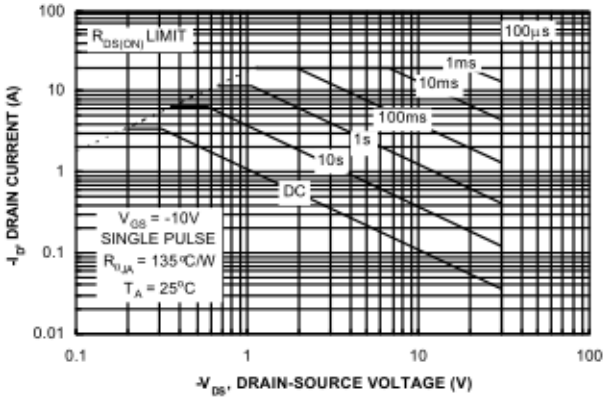


Figure 9. Maximum Safe Operating Area.

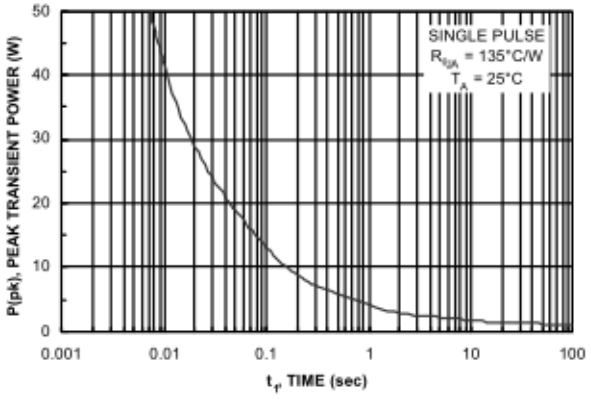


Figure 10. Single Pulse Maximum Power Dissipation.

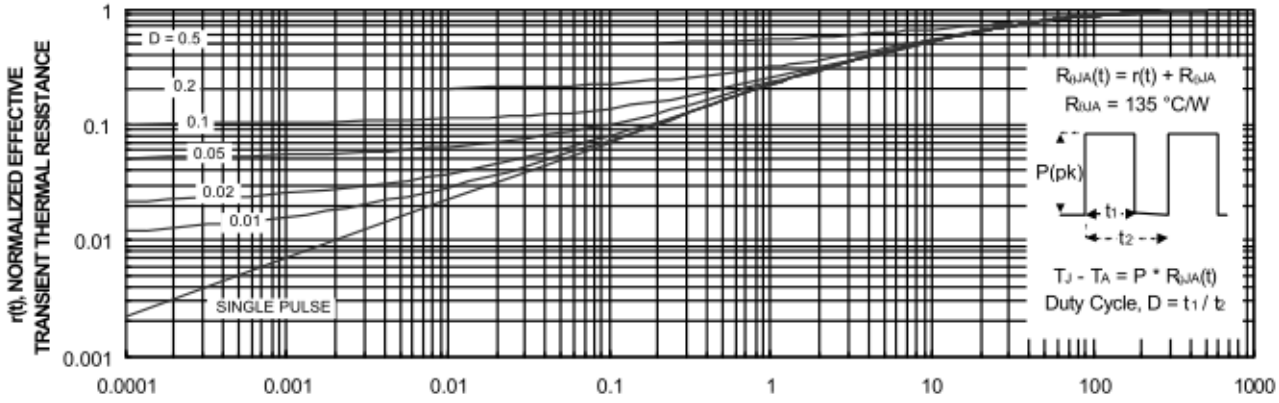


Figure 11. Transient Thermal Response Curve.