

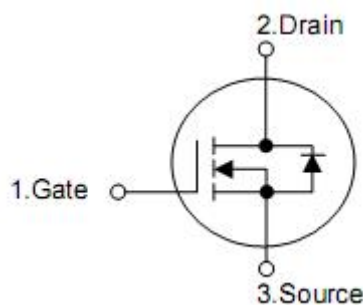
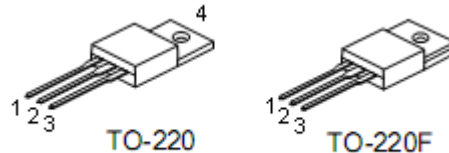
1. Description

The KNX6165A-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology

2. Features

- n ROHS Compliant
- n $R_{DS(ON),typ}=0.6 \Omega @ V_{GS}=10V$
- n Low Gate Charge Minimize Switching Loss
- n Fast Recovery Body Diode

3. Pin configuration



Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Ordering Information

Part Number	Package	Brand
KNF6165A	TO-220F	KIA
KNP6165A	TO-220	KIA

5. Absolute maximum ratings

TC=25°C unless otherwise specified

Parameter	Symbol	Ratings		Unit
		TO220	TO220F	
Drain-to-Source Voltage	V_{DSS}	650		V
Gate-to-Source Voltage	V_{GSS}	±20		
Continuous Drain Current	I_D	10		A
Pulsed Drain Current at $V_{GS}=10V$	I_{DM}	40		
Single Pulse Avalanche Energy	E_{AS}	800		mJ
Power Dissipation	P_D	216	50	W
Derating Factor above 25 °C		1.72	0.4	W/ °C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	T_L T_{PAK}	300		°C
Operating and Storage Temperature Range	T_J & T_{STG}	-55 to 150		

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Ratings		Units
		TO220	TO220F	
Thermal resistance, junction-ambient	$R_{\theta JA}$	62	100	°C/W
Thermal resistance, Junction-case	$R_{\theta JC}$	0.58	2.5	

7. Electrical characteristics

(T_J=25°C, unless otherwise notes)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Off characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	650	-	-	V
Drain-to-source Leakage Current	I _{DSS}	V _{DS} =650, V _{GS} =0V	-	-	1	μA
		V _{DS} =520, V _{GS} =0V T _J =125°C,	-	-	100	μA
Gate-body leakage current	I _{GSS}	V _{GS} =20V, V _{DS} =0V	-	-	+1.0	nA
		V _{GS} =-20V, V _{DS} =0V	-	-	-1.0	nA
On characteristics						
Static drain-source on-resistance	R _{DS(on)}	V _{GS} =10V, I _D =5A	-	0.6	0.9	Ω
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0	-	4.0	V
Forward Transconductance	g _{fs}	V _{DS} =15V, I _D =5A	-	10	-	S
Dynamic characteristics						
Input capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHz	-	1554	-	pF
Output capacitance	C _{oss}		-	153	-	pF
Reverse transfer capacitance	C _{rss}		-	15	-	pF
Total gate charge						
Turn-on delay time	t _{d(on)}	V _{DD} =325, I _D =10A, V _{GS} =10V, R _G =9.1Ω	-	15	-	ns
Rise time	t _r		-	25	-	ns
Turn-off delay time	t _{d(off)}		-	51	-	ns
Fall time	t _f		-	31	-	ns
Total gate charge	Q _g	V _{DS} =325V, I _D =10A, V _{GS} =0 to 10V	-	39	-	nC
Gate-source charge	Q _{gs}		-	7.0	-	nC
Gate-drain charge	Q _{gd}		-	16	-	nC
Drain-source diode characteristics						
Drain-source diode forward voltage	V _{SD}	V _{GS} =0V, I _S =10A	-	-	1.5	V
Continuous drain-source current ^[2]	I _{SD}	Integral pn-diode In MOSFET	-	-	10	A
Pulsed drain-source current ^[2]	I _{SM}		-	-	40	A
Reverse recovery time	t _{rr}	V _{GS} =0V, I _F =10A	-	273	-	ns
Reverse recovery charge	Q _{rr}	dI _{SD} /dt=100A/μs	-	1.7	-	μC

Note: [1] T_J=+25 °C to +150 °C

[2] Pulse width≤380μs; duty cycle≤2%.

8. Typical Characteristics

Figure 1. Output Characteristics ($T_J = 25^\circ\text{C}$)

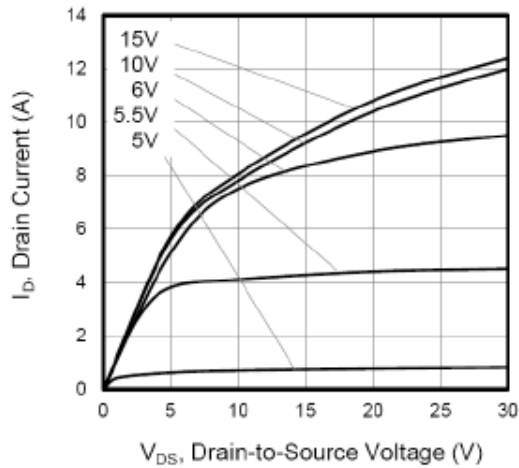


Figure 2. Forward Bias Safe Operating Area

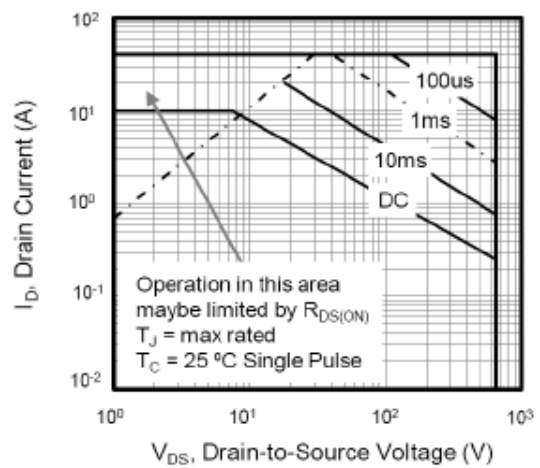


Figure 3. Drain Current vs. Temperature

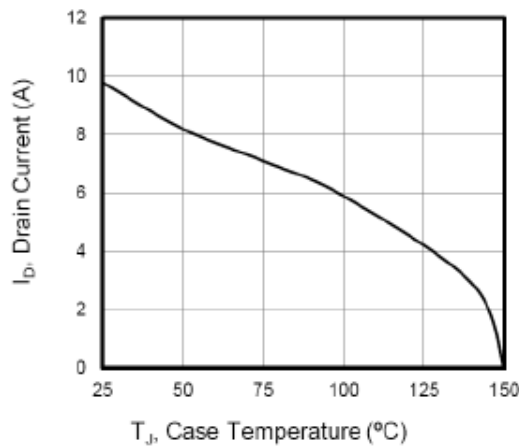


Figure 4. BV_{DSS} Variation vs. Temperature

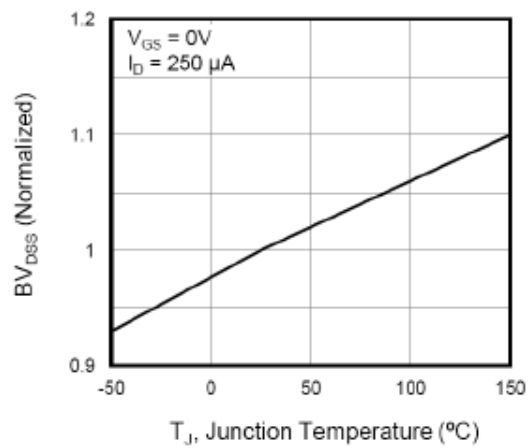


Figure 7. Capacitance

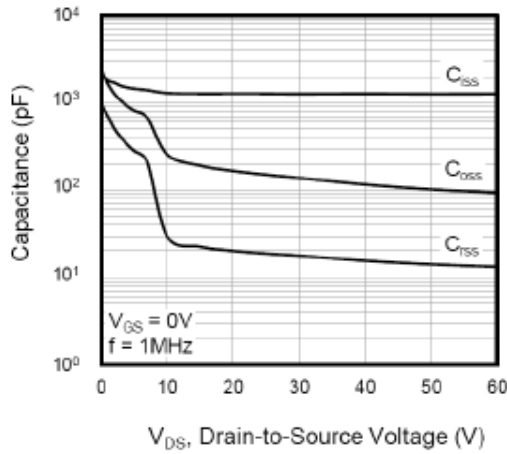


Figure 8. Gate Charge

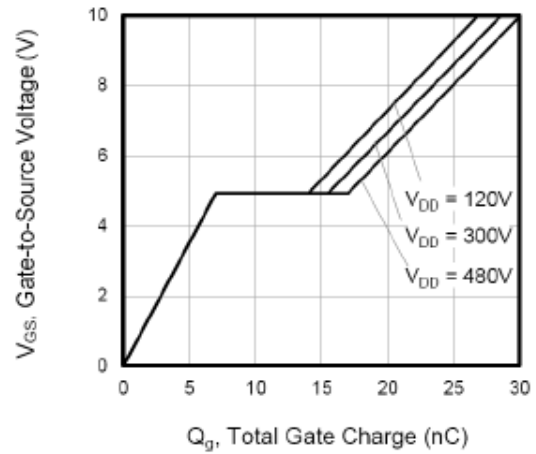


Figure 9. Body Diode Forward Voltage

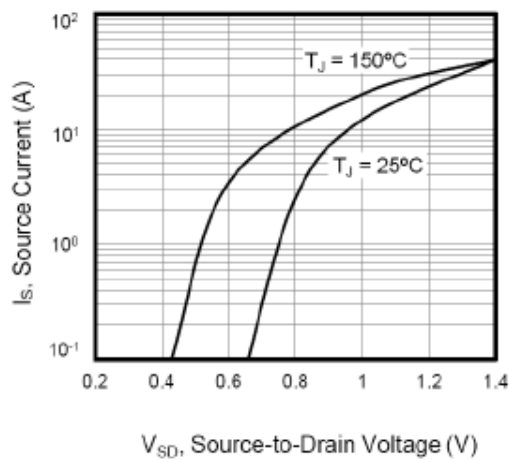
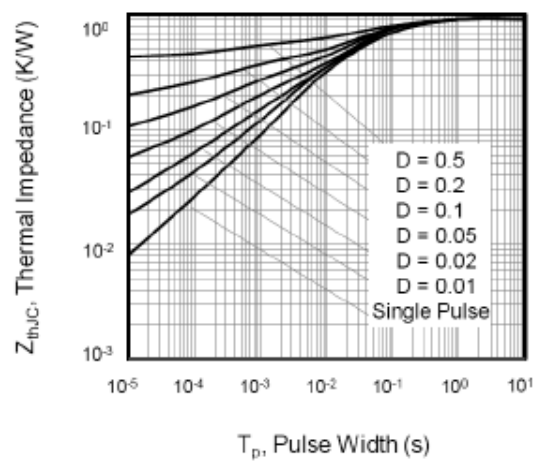


Figure 10. Transient Thermal Impedance



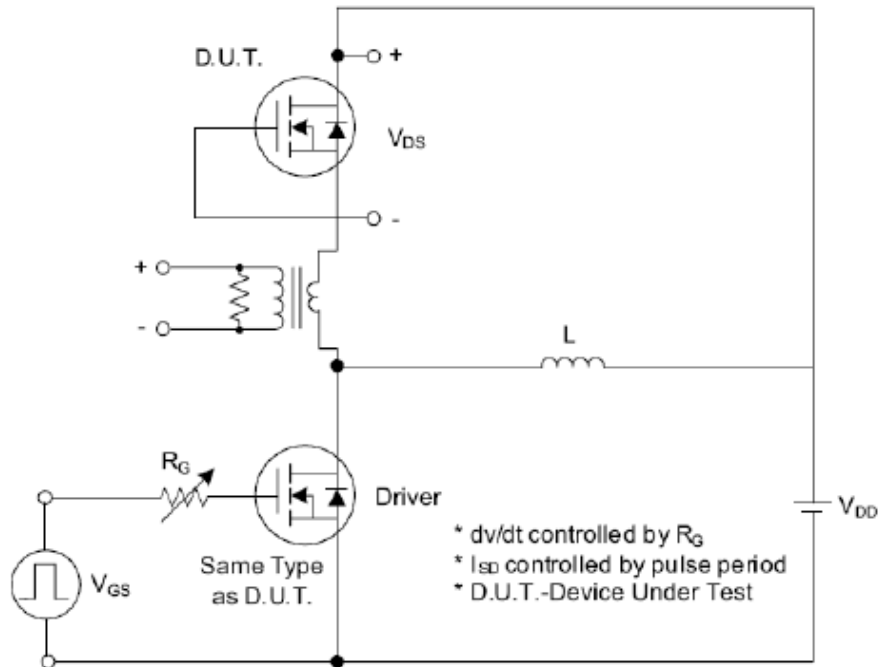


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

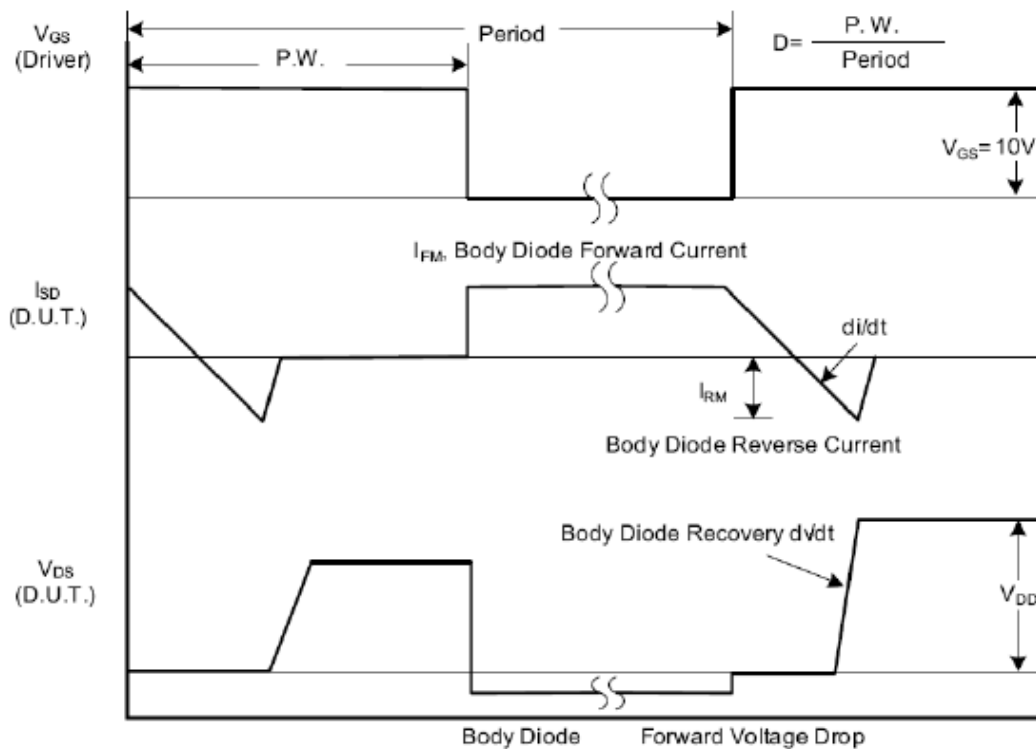


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

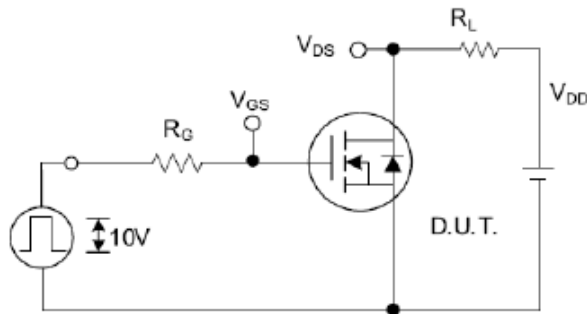


Fig. 2.1 Switching Test Circuit

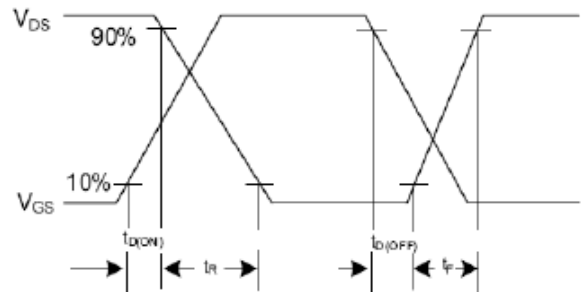


Fig. 2.2 Switching Waveforms

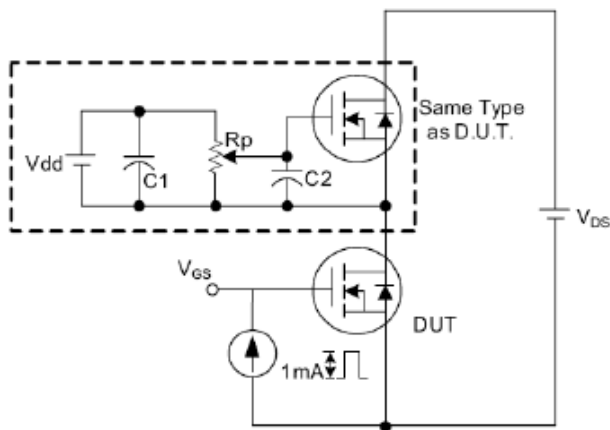


Fig. 3.1 Gate Charge Test Circuit

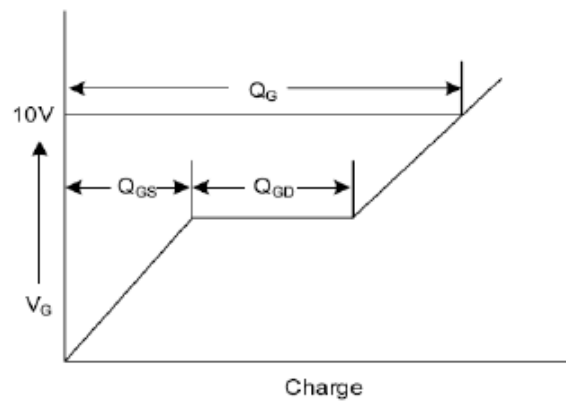


Fig. 3.2 Gate Charge Waveform

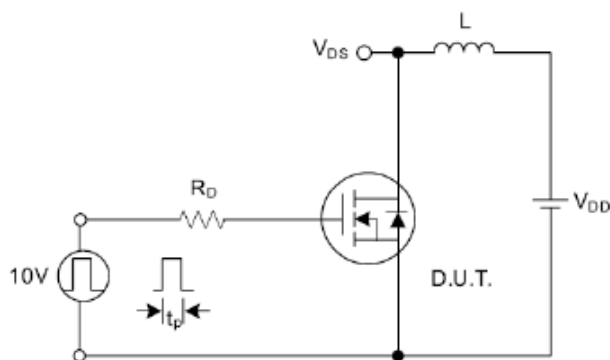


Fig. 4.1 Unclamped Inductive Switching Test Circuit

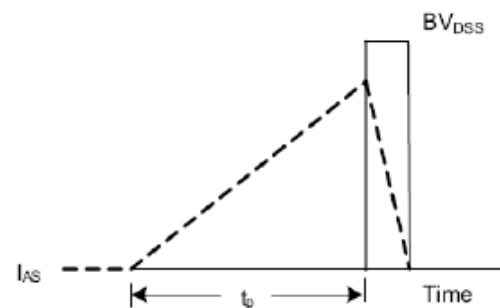


Fig. 4.2 Unclamped Inductive Switching Waveforms