

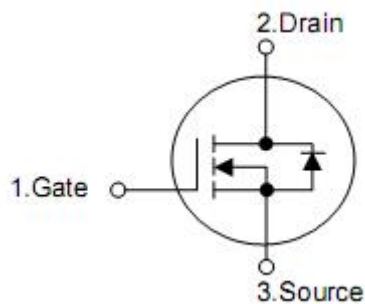
1. Description

The KND3404C is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The KND3404C meet the RoHs and Green Product requirement 100% EAS Guaranteed with full function reliability approved.

2. Features

- n $R_{DS(ON),typ.}=5.0m\Omega@V_{GS}=10V$
- n Super low gate charge
- n 100% EAS Guaranteed
- n Green device available
- n Excellent Cdv/dt effect decline
- n Advanced high cell density trench technology

3. Symbol



Pin TO-252	Pin DFN5*6	Function
1	4	Gate
2	5,6,7,8	Drain
3	1,2,3	Source

4. Ordering Information

Part Number	Package	Brand
KND3404C	TO-252	KIA
KNY3404C	DFN5*6	KIA

5. Absolute maximum ratings

(T_A=25°C, unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-source voltage	V _{DS}	40	V
Gate-source voltage	V _{GS}	±20	V
Continuous drain current V _{GS} @10V ¹	T _C =25°C	I _D	80
	T _C =100°C	I _D	58
Pulsed drain current ²	I _{DM}	150	A
Single pulse avalanche energy ³	EAS	110	mJ
Avalanche current	I _{AS}	47	A
Total power dissipation ⁴	T _C =25°C	P _D	52.1
Junction and storage temperature range	T _J , T _{STG}	-55 to 150	°C

6. Thermal Data

Parameter	Symbol	Ratings	Units
Thermal resistance, junction-ambient	R _{thJA}	62	°C/W
Thermal resistance, Junction-case	R _{thJC}	2.4	°C/W

7. Electrical characteristics

($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40	--	--	V
BVDSS Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference to 25°C , $I_D=1\text{mA}$	--	0.034	--	$\text{V}/^{\circ}\text{C}$
Static Drain-Source On-Resistance ²	$R_{DS(ON)}$	TO-252 $V_{GS}=10V, I_D=15A$ DFN5*6 $V_{GS}=10V, I_D=10A$	--	5.0	6.5	$\text{m}\Omega$
		TO-252 $V_{GS}=4.5V, I_D=12A$ DFN5*6 $V_{GS}=4.5V, I_D=5A$	--	6.5	9	$\text{m}\Omega$
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	--	2.5	V
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	--	-5.84	--	$\text{mV}/^{\circ}\text{C}$
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=32V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	--	---	1	μA
		$V_{DS}=32V, V_{GS}=0V, T_J=55^{\circ}\text{C}$	--	---	5	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	--	---	± 100	nA
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=15A$	--	25	---	S
Gate Resistance	R_g	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	--	1.5	---	Ω
Total Gate Charge (4.5V)	Q_g	$V_{DS}=20V, V_{GS}=4.5V, I_D=12A$	--	28	---	nC
Gate-Source Charge	Q_{gs}		--	7.8	---	nC
Gate-Drain Charge	Q_{gd}		--	12.5	---	nC
Turn-On Delay Time	$T_{d(on)}$	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega, I_D=1A$	--	20	---	ns
Rise Time	T_r		--	11.5	---	ns
Turn-Off Delay Time	$T_{d(off)}$		--	84	---	ns
Fall Time	T_f		--	8.5	---	ns
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	--	3330	---	pF
Output Capacitance	C_{oss}		--	270	---	pF
Reverse Transfer Capacitance	C_{rss}		--	200	---	pF
Diode Characteristics						
Continuous Source Current ^{1,5}	I_S	$V_G=V_D=0V, \text{Force Current}$	--	--	80	A
Pulsed Source Current ^{2,5}	I_{SM}		--	--	150	A
Diode Forward Voltage ²	V_{SD}	$V_{GS}=0V, I_S=1A, T_J=25^{\circ}\text{C}$	--	--	1	V

Note:1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.

2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

3. The EAS data shows Max.rating. The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=47A$.

4. The power dissipation is limited by 150°C junction temperature.

5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation

8. Test circuits

Typical Characteristics

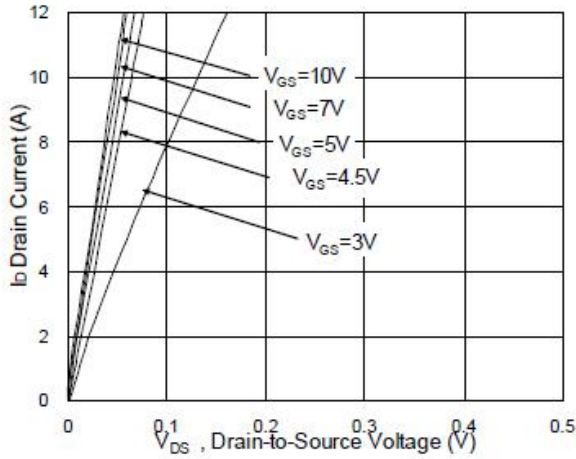


Fig.1 Typical Output Characteristics

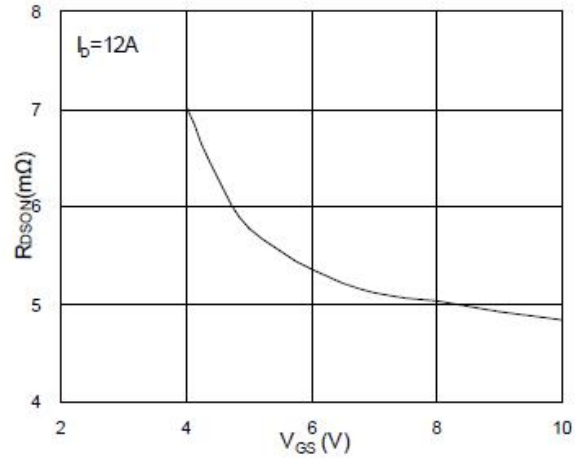


Fig.2 On-Resistance vs. G-S Voltage

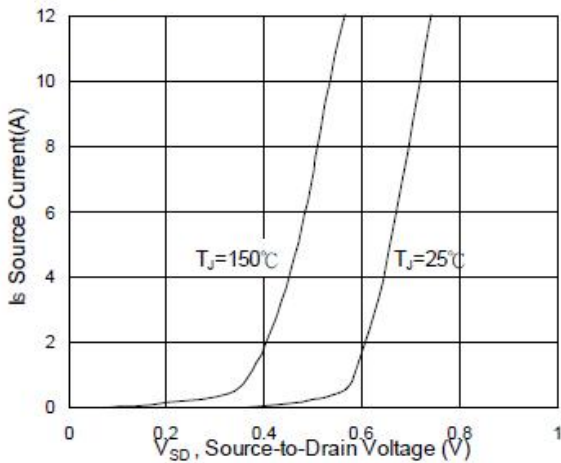


Fig.3 Forward Characteristics Of Reverse

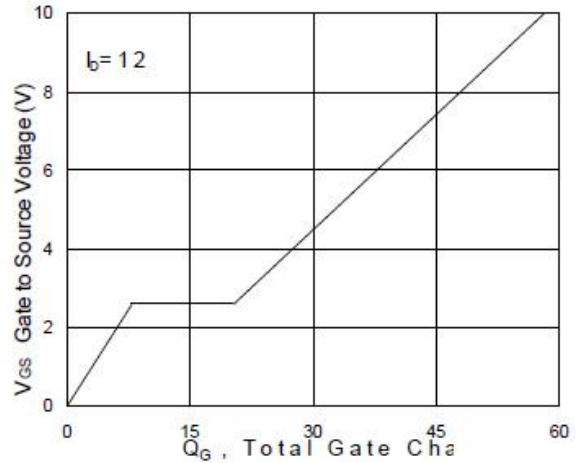


Fig.4 Gate-Charge Characteristics

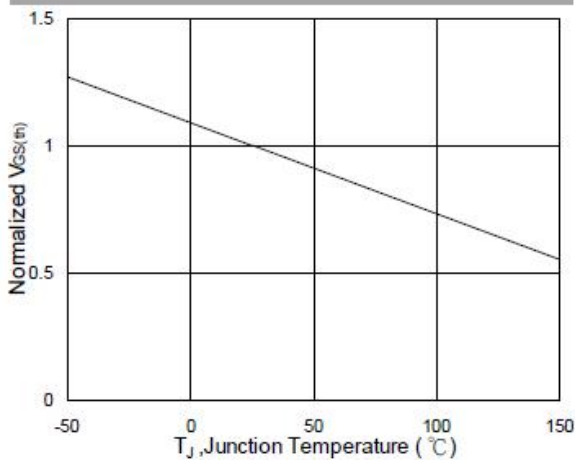


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

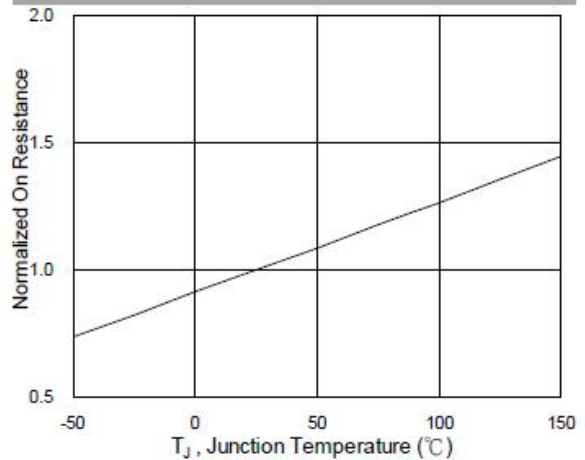


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

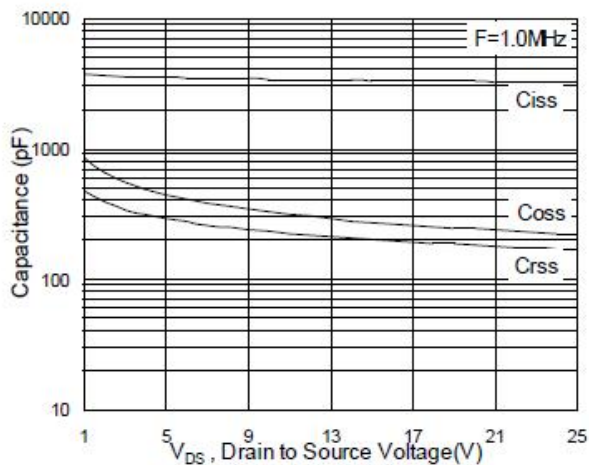


Fig.7 Capacitance

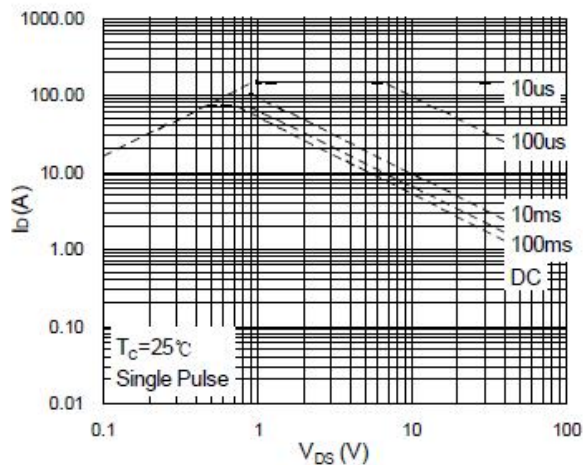


Fig.8 Safe Operating Area

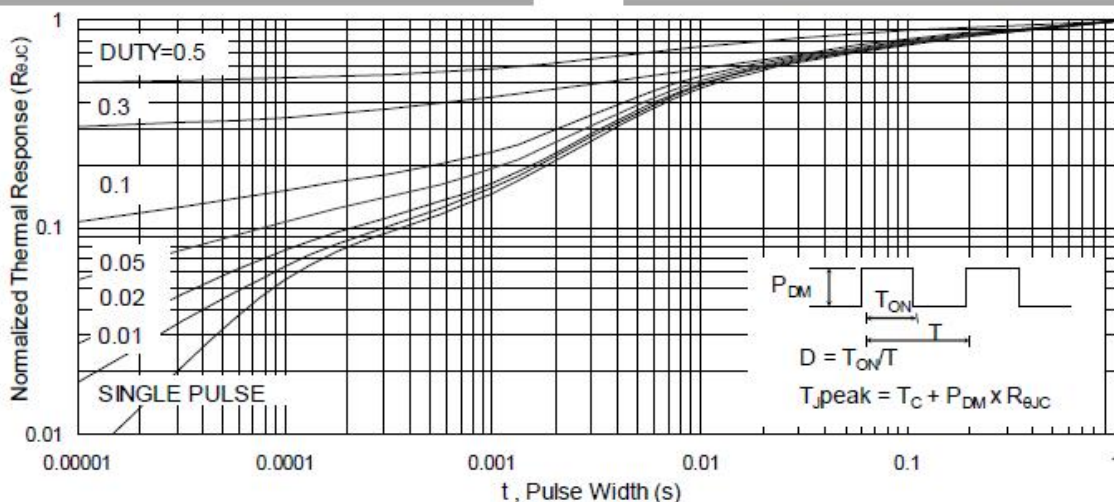


Fig.9 Normalized Maximum Transient Thermal Impedance

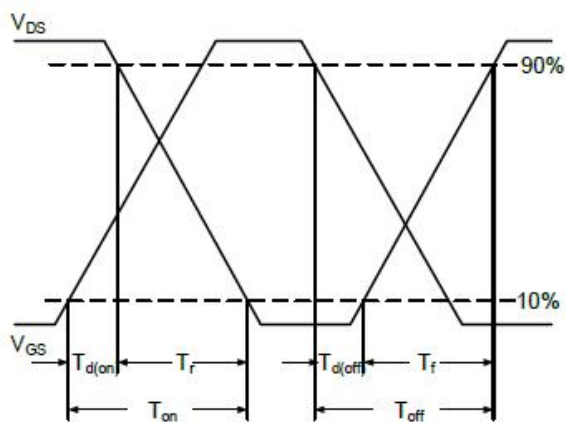


Fig.10 Switching Time Waveform

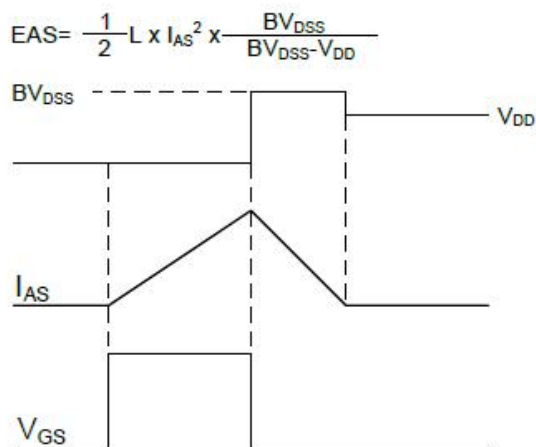


Fig.11 Unclamped Inductive Switching Wave